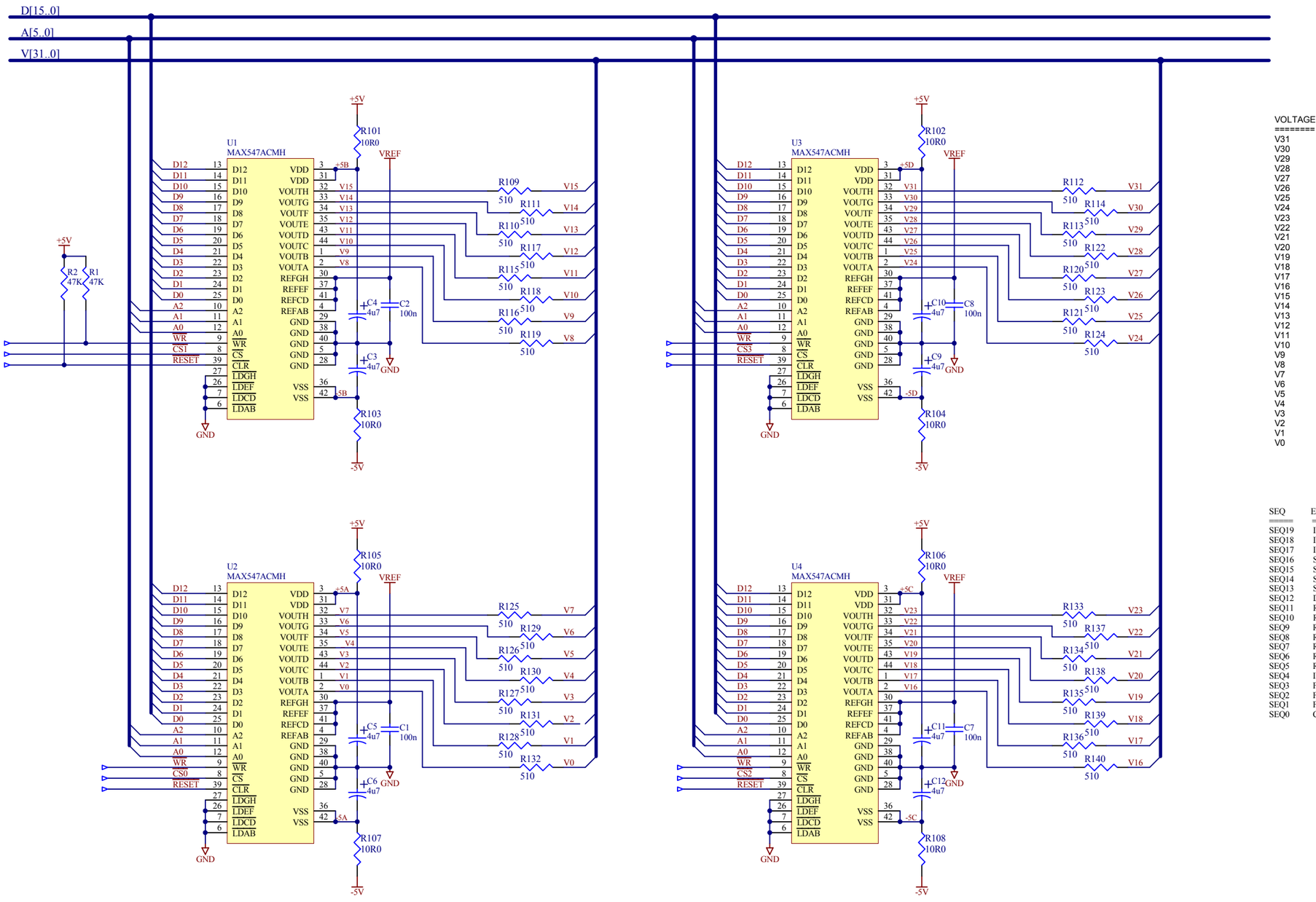


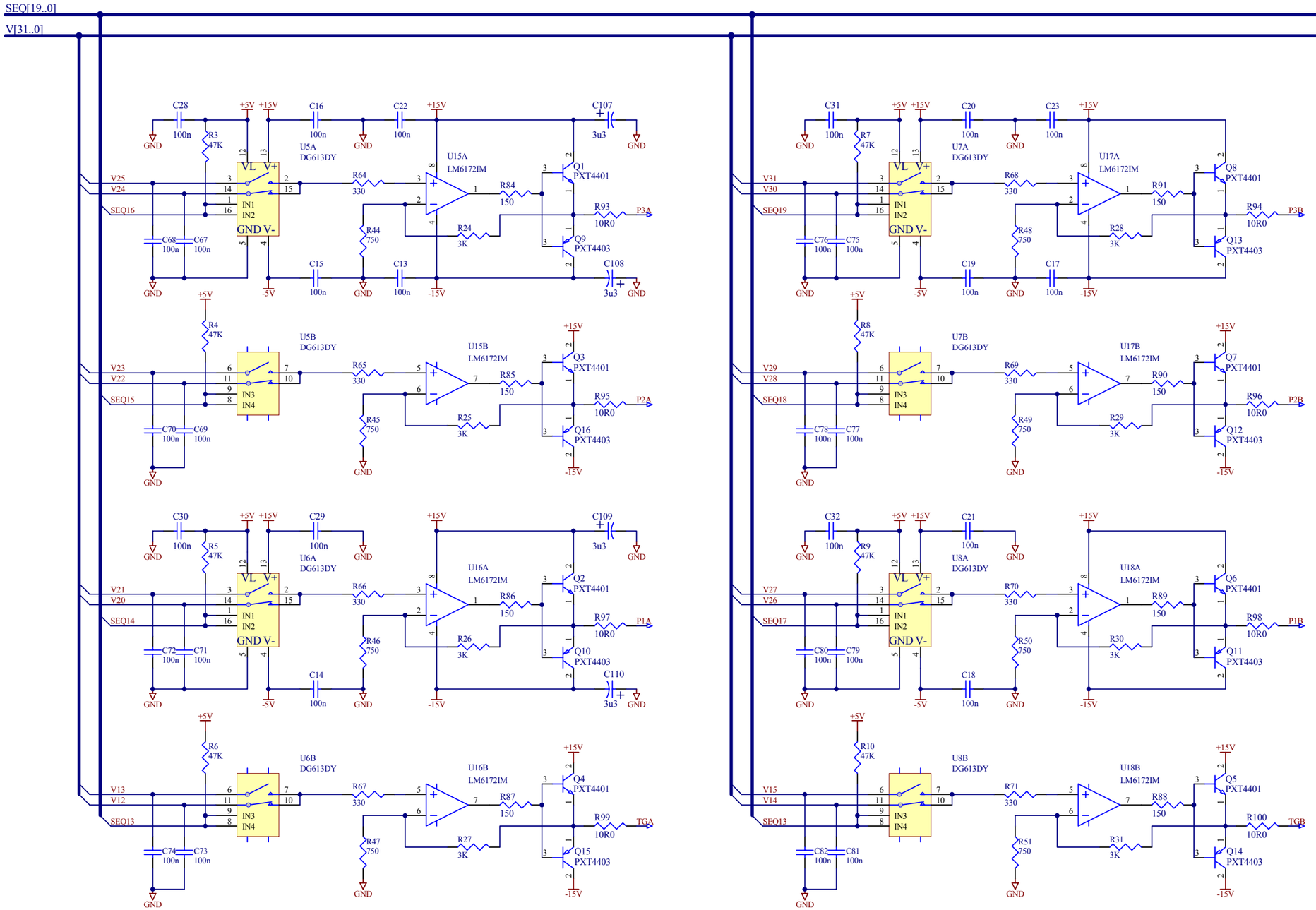
VOLTAGE	SLOT
V31	P3_B+
V30	P3_B-
V29	P2_B+
V28	P2_B-
V27	P1_B+
V26	P1_B-
V25	P3_A+
V24	P3_A-
V23	P2_A+
V22	P2_A-
V21	P1_A+
V20	P1_A-
V19	S_B+
V18	S_B-
V17	S_A+
V16	S_A-
V15	TG_B+
V14	TG_B-
V13	TG_A+
V12	TG_A-
V11	SW_B+
V10	SW_B-
V9	SW_A+
V8	SW_A-
V7	RG_B+
V6	RG_B-
V5	RG_A+
V4	RG_A-
V3	IPC_B+
V2	IPC_B-
V1	IPC_A+
V0	IPC_A-

SEQ	EEV	SITE
SEQ19	IM3	P3B
SEQ18	IM2	P2B
SEQ17	IM1	P1B
SEQ16	ST3	P3A
SEQ15	ST2	P2A
SEQ14	ST1	P1A
SEQ13	SPARE	TG
SEQ12	DG	SW
SEQ11	R3L	S3B
SEQ10	R2L	S2B
SEQ9	R1L	S1B
SEQ8	R3R	S3A
SEQ7	R2R	S2A
SEQ6	R1R	S1A
SEQ5	RG	RG
SEQ4	IPC	IPC
SEQ3	FINT+	FINT+
SEQ2	FINT-	FINT-
SEQ1	FRST	FRST
SEQ0	CONVST	CONVST

Title
BASE CLOCK DRIVER PCB

Revision: 2.1a
Date: 7/1/2005
Sheet 1 of 5
File: C:\base\clkdrv_v2\clkdrvA.SchDoc

OCIW
813 Santa Barbara Street
Pasadena, CA 91101
www.ociw.edu

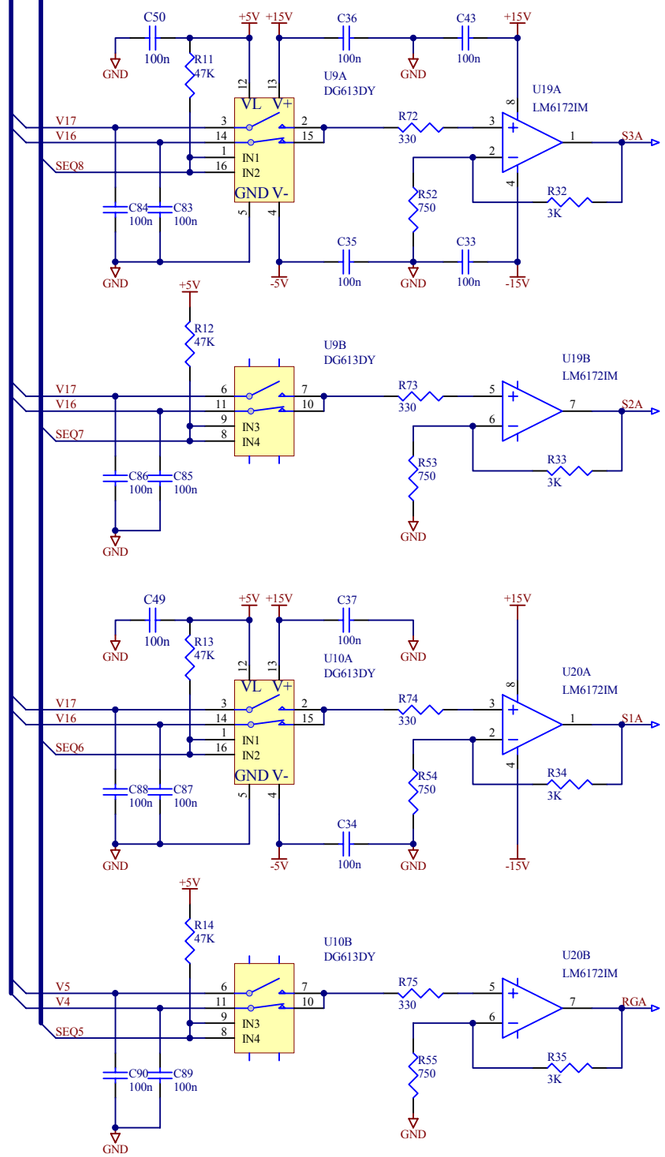


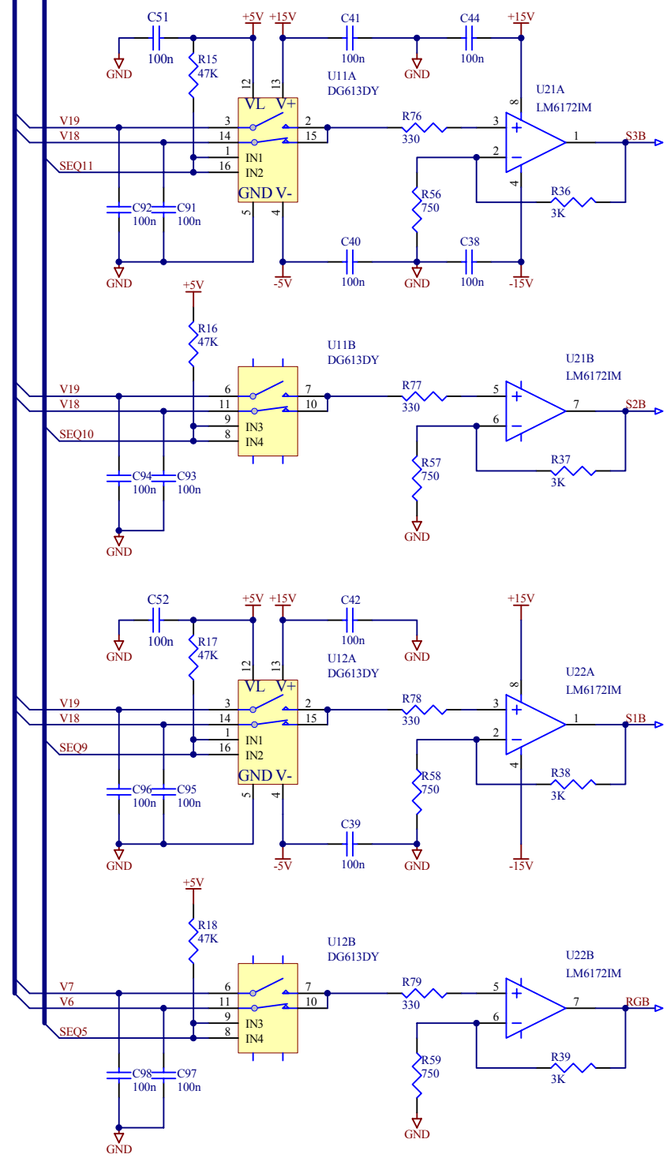
GAIN = 5 OUTPUT = 5 mV/DN

Title: **BASE CLOCK DRIVER PCB**		*OCIW* *813 Santa Barbara Street* *Pasadena, CA 91101* *www.ociw.edu*
Revision: 2.1a	Date: 7/1/2005	
Sheet 2 of 5	File: C:\base\clkdrv_v2\clkdrvB.SchDoc	

SEQ[19..0]

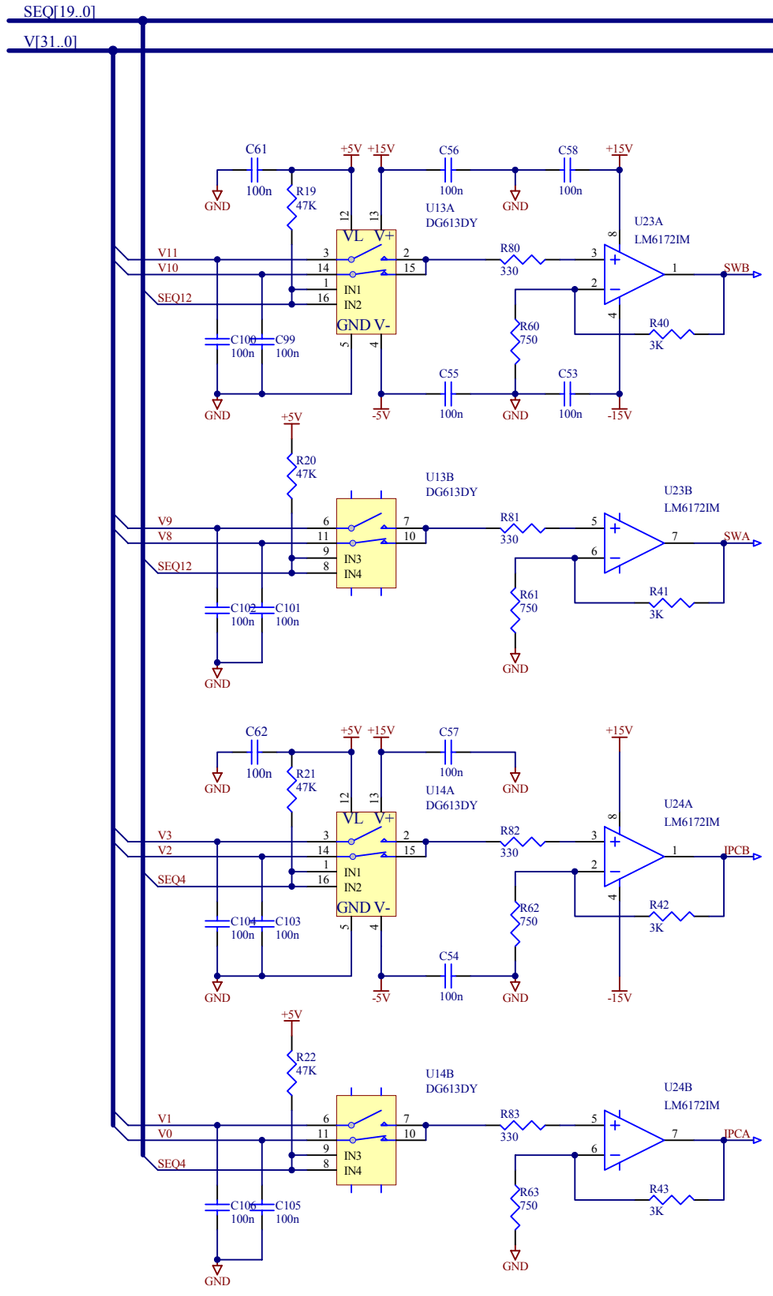
V[31..0]





GAIN = 5 OUTPUT = 5 mV/DN

Title: **BASE CLOCK DRIVER PCB**		*OCIW* *813 Santa Barbara Street* *Pasadena, CA 91101* *www.ociw.edu*
Revision: 2.1a	Date: 7/1/2005	
Sheet 3 of 5	File: C:\base\clkdrv_v2\clkdrvC.SchDoc	



GAIN = 5 OUTPUT = 5 mV/DN

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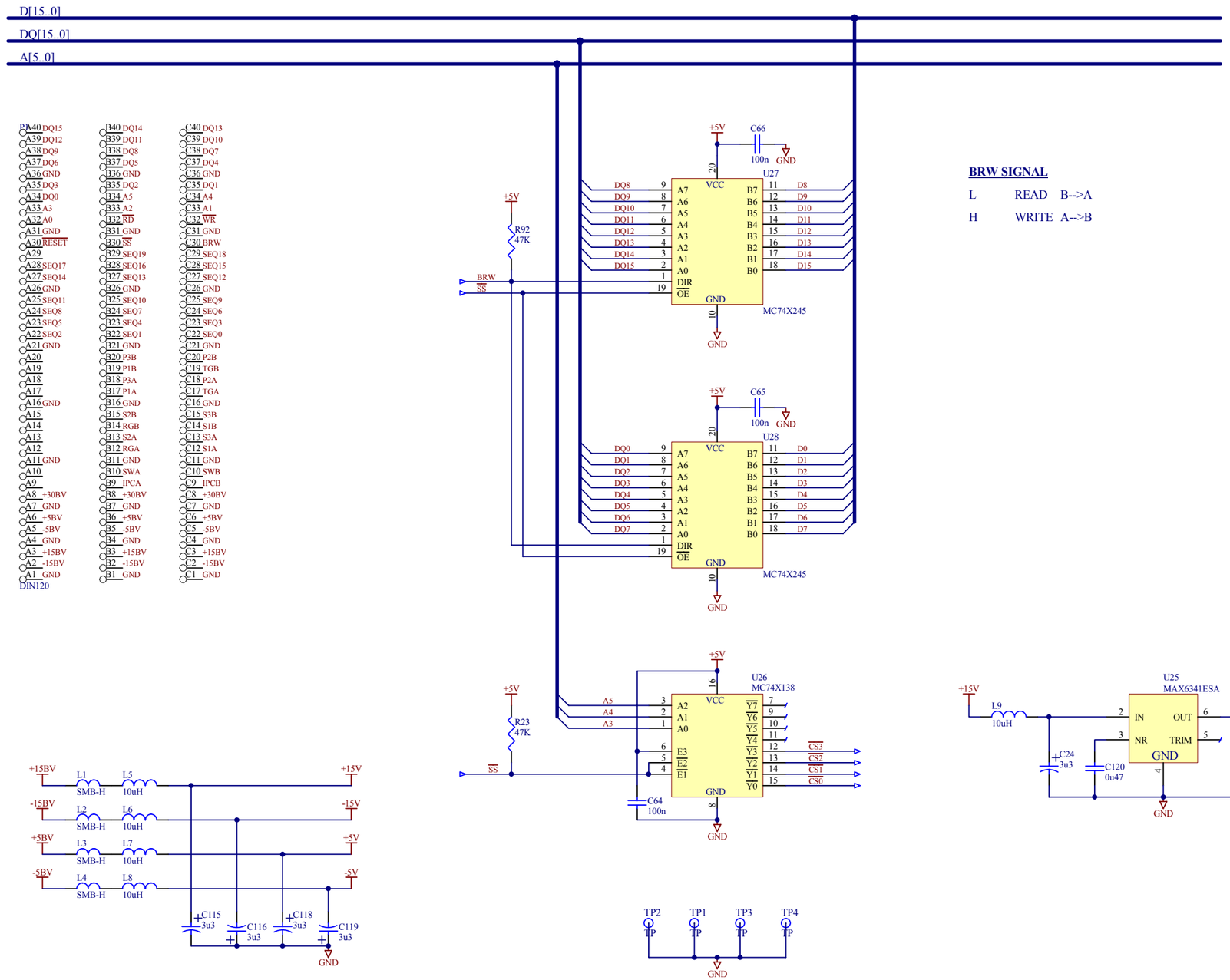
Revision: 2.1a	Date: 7/1/2005	
Sheet 4 of 5	File: C:\base\clkdrv_v2\clkdrvD.SchDoc	



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Revision:	2.1a	Date: 7/1/2005	
Sheet	5 of 5	File: C:\base\clkdrv_v2\clkdrvE.SchDoc	