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A Versatile CCD Wave Front Curvature Sensor

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ABSTRACT. Small-format CCD detectors are well suited to wave front sensing applications. The prototype wave front sensor described here is based on a low-noise frame transfer 64 × 64 device with a DSP56002-based controller. The subaperture patterns necessary for curvature sensing are formed by extensive serial register binning. The reduced number of pixels allows rapid frame rates with low readout noise. The CCD is thermoelectrically cooled to minimize dark current. Versatility is achieved by having the serial binning pattern and the number of subapertures under software control.

1. INTRODUCTION

In an adaptive optics system, the distortion of an incoming wave front by thermal turbulence in the atmosphere is detected by a wave front sensor and then corrected by a deformable mirror. In one technique, the variation in wave front curvature is sensed from out-of-focus image(s) of a guide star (Roddier 1988; Roddier, Roddier, & Roddier 1988; Hickson 1994). The dwell time of the wave front distortions is typically ~10 ms, which means that the sensor must be read out even more frequently. In order to use guide stars that are as faint as possible, the wave front sensor must have high quantum efficiency, a wide dynamic range, and low intrinsic noise. To sample the turbulence bandwidth adequately, shutterless operation is much preferred, while the spatial sampling must be adequate for the subaperture patterns. It must also be possible to calibrate the device easily and readily integrate it into the optical system.

Small-format CCD detectors meet these requirements very well. Current technology allows high quantum efficiency devices with rapid readout and frame transfer. Serial register binning reduces the number of pixels for low-noise operation at rapid frame rates. A frame transfer architecture allows the source to be almost continuously monitored and provides shutterless operation. Ease of implementation and alignment in an optical system makes the simplicity of a CCD appealing.

Our prototype wave front sensor was constructed using a low-noise frame transfer 64 × 64 CCD with a digital signal processor (DSP)–based CCD controller. Figure 1 is a block diagram that shows the various parts of the sensor system. The controller provides bias voltages, three phase clock signals to the parallel and serial registers, signal processing to extract and digitize the CCD output signal, and a fast serial interface to a host computer.

For curvature sensing, the image of the guide star on the CCD is divided into a number of subapertures, as shown in Figure 2. The key to a practical sensor is to read the array by binning the serial register on a line-by-line basis according to the subaperture pattern, so that the number of "superpixels" read is a minimum. This approach permits low-noise readout with fast frame rates. Initial 2 × 2 binning of the 64 × 64 device reduces the number of pixels to be read to 1024. Further superpixel binning in the serial register during readout reduces the number of read operations to about 200. The number of pixels per superpixel depends on the line of the CCD being read and on the pattern being sampled.

While there are many existing CCD controller designs, not all would be suitable for operating a small frame transfer CCD as a wave front sensor. Some of these demonstrate useful features such as software programmability, numerous clock signals, fast clock rates, multiple amplifier gain settings, and operating point voltages controllable over a very wide range (Reiss 1994; Doherty, Sutcliffe, & Sims 1992). Others are optimized for low-noise performance at slow scan rates (Johnson 1988) or bare simplicity (Chen & Novello 1989; Gillam, Johnson, & Smith 1992). The prototype controller we have designed and built for this project is an attempt to synthesize the key elements into one design. A high level of integration is achieved by the extensive use of a DSP and its peripherals, eliminating external sequencers and state machines, wait state generators, clocks, and counters found in other designs. Some features of the various designs such as dual-speed readout, operation of multiple devices, expansion beyond four amplifiers, fiber optic data links, and VME–based data interfaces are not included in order to simplify the hardware design. Some timing and software complications are avoided by excluding features such as directly writing the clock waveforms to high-speed digital-to-analog converters (Leach 1988) for each clock transition.

For the prototype sensor, a digital signal processor–based controller delivers the flexibility and computational power required to perform the serial register binning, to adapt to dif-

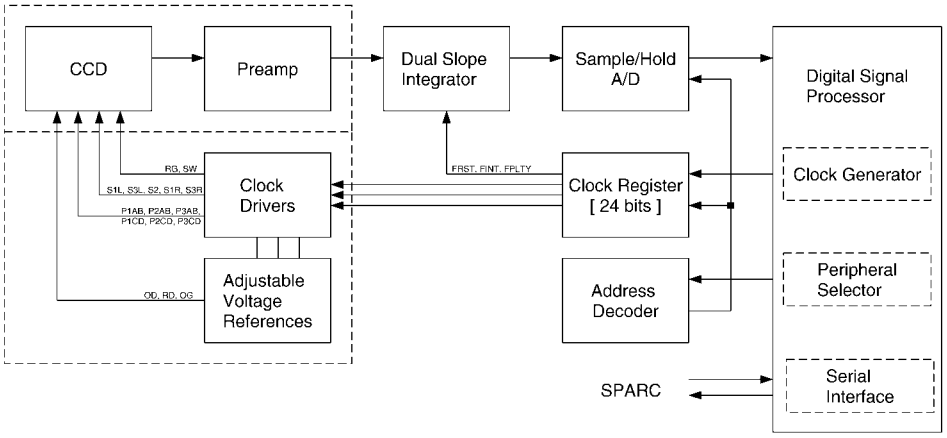

FIG. 1.—Block diagram of the AO system. The digital signal processor generates the clock signals, controls the dual-slope integrator, and reads the digitized data.

ferent subaperture patterns through software control, and to extract the curvature signal from the sensor image. Versatile and programmable clock sequencing and low-noise operation were the main design requirements. The DSP directly generates the sequences used to clock the serial and parallel charge transfers on the CCD. Extra clock lines are provided for frame transfer and split serial register operation. The DSP also controls the dual slope integrator and accepts the filtered and digitized output from the A/D converters. The design of the dual-slope integrator and clock drivers borrows some details from previous University of British Columbia efforts (Johnson 1988).

2. FRAME TRANSFER CCD

The prototype CCD wave front curvature sensor uses a 64 × 64 frame transfer device designed by J. Geary and fabricated by Loral on a joint UBC-SAO wafer run. The 64 × 128 array is made up of four sections of 64 × 32 pixels, each independently clocked (as shown in Fig. 3). Each end of the device has a split serial register with two output amplifiers. The device is frontside illuminated, with 15 μm square pixels and less than 10 e^- rms readout noise.

The frame transfer architecture allows fast frame rates while providing a readout rate consistent with low read noise performance. At the end of each integration time, the recorded image charge is rapidly shifted from the illuminated area to the readout area of the device. Provided this transfer is fast compared to the integration time, a reasonable extinction ratio is maintained, and a shutter is not required. We chose to illuminate on one half (64 × 64) with frame transfer to the other side, although it could also be illuminated on the central 64 × 64 pixels with frame transfer to the 64 × 32 areas at each end for readout using all four output amplifiers.

In order to reduce the dark current and to allow the CCD amplifiers to operate with lower thermal noise, the CCD is thermoelectrically (TE) cooled within a dry gas-filled housing. At room temperature, the measured dark current of 120 pA cm^{-2} is noticeable even in short (10 ms) exposures. At a target operating temperature of −40°C, the dark current is reduced to less than 1/10th electron per 10 ms exposure per pixel. An adjustable current source provides the current driven through the TE cooler, which is rated for $\Delta T = 77$°C under ideal no-load conditions with a current of 1.2 A (Marlow Industries 1990). A platinum resistive sensor in contact with the TE cooler cold side monitors the temperature of the CCD, while a water-cooled heat sink bolted to the housing base plate removes the heat from the TE cooler hot side. Even at low flow rates, the entire CCD housing and mounting bracket can be rapidly chilled to the water temperature (nominally 10°C at the telescope).

Two low-noise preamplifiers are located inside the Dewar close to the CCD to minimize noise pickup. The CCD is clamped into a socket on the header circuit board in contact with the TE cooler cold side. The header board is supported by stainless steel standoffs. Low thermal conductivity Constantan wires connect the CCD inputs and preamplifier outputs to the electrical connectors. Figures 4*a* and 4*b* are photographs of the wave front sensor showing these features.

3. DSP DESCRIPTION AND CLOCK GENERATION

The versatility of the controller stems from the use of a Motorola 24 bit DSP56002 digital signal processor (Motorola 1992). On-chip resources permit the DSP to run code from an internal program memory and to use two internal data memories for storage. External 32 K SRAM memory is available as necessary. The DSP runs at a clock frequency of 40 MHz and has a 50 ns instruction cycle. DSP instructions are typically executed in one cycle. The speed of the processor allows the CCD clocking sequences to be directly generated by the DSP under program control, which ensures versatility of the se-

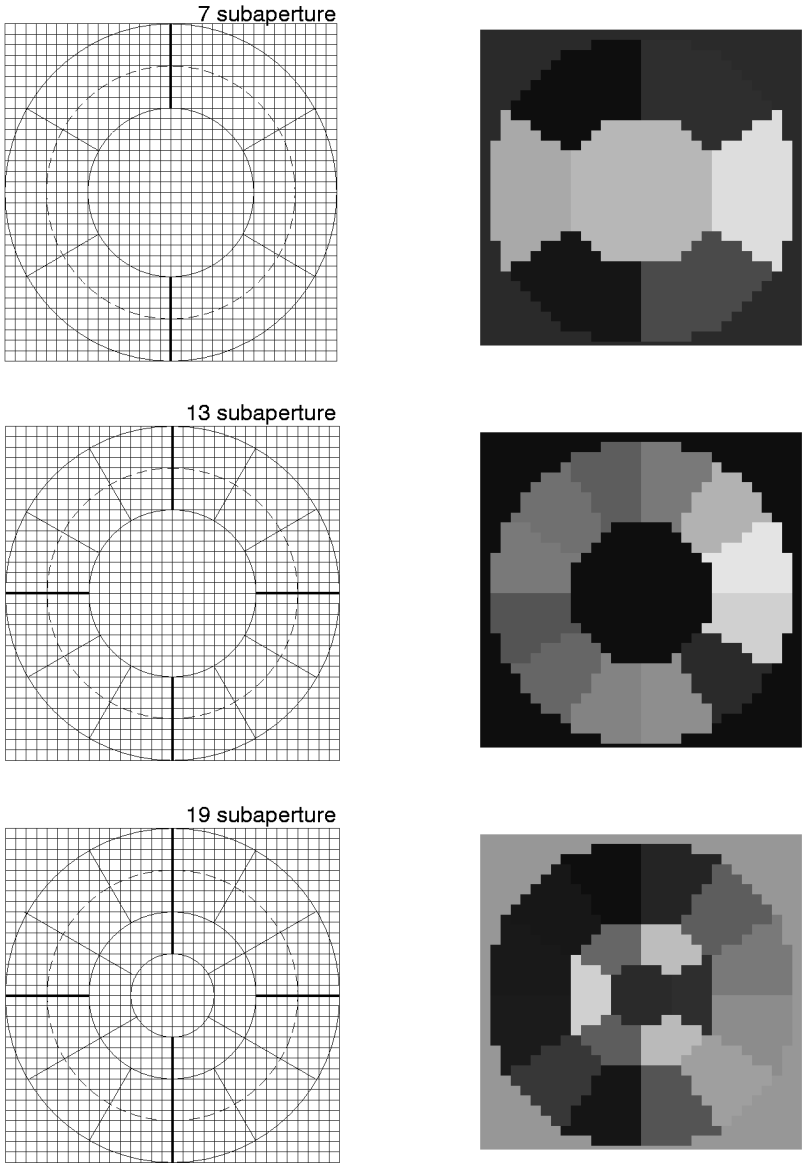

FIG. 2.—Sample readout patterns. The defocused guide star image can be sampled with various subaperture patterns through software configuration of the CCD readout. The dashed circle represents the outline of the spot produced by the defocused beam. Each of the boundary subapertures extends beyond the beam to provide tip-tilt information. Wave front sensor images (*right*) are 10 ms exposures taken in the lab showing the corresponding programmed subaperture patterns.

quencing. Communication with a host SPARC processor is available via both a fast SBus serial link and a slower RS-232 monitor channel, using on-chip DSP peripherals.

In order to perform the serial and parallel charge transfers on the CCD, the clock signals are generated by the DSP from sequence fragments stored in its on-chip data memory. A typical timing diagram and the sequence fragments used to produce it are shown in Figures 5*a* and 5*b*. Each bit of the 24 bit DSP word represents one of the control signals. With 24 bits, there are control signals for the two sets of parallel clocks necessary for frame transfer (P1AB-P2AB-P3AB, P1CD-P2CD-P3CD) and the two sets of serial clocks necessary to use amplifiers at each end of the serial register (S1R-S3R-S2-S1L-S3L-RG). Other signals control the pixel conversion functions such as the dual slope integrator on/off and polarity, integrator capacitor reset, and A/D converter start ($\overline{\text{FINT}}$, FPLTY, $\overline{\text{FRST}}$, $\overline{\text{CONVST}}$). Spare bits allow additional signals for a summing well, transfer gate, or a shutter to be added.

To perform an operation such as a serial or parallel shift, the DSP steps though and writes the sequence of data words into an external 24 bit register via the DSP external bus. Each sequence fragment is held in the external register until it is overwritten by the next fragment after a preset number of clock cycles, as coded into the DSP control software. The number

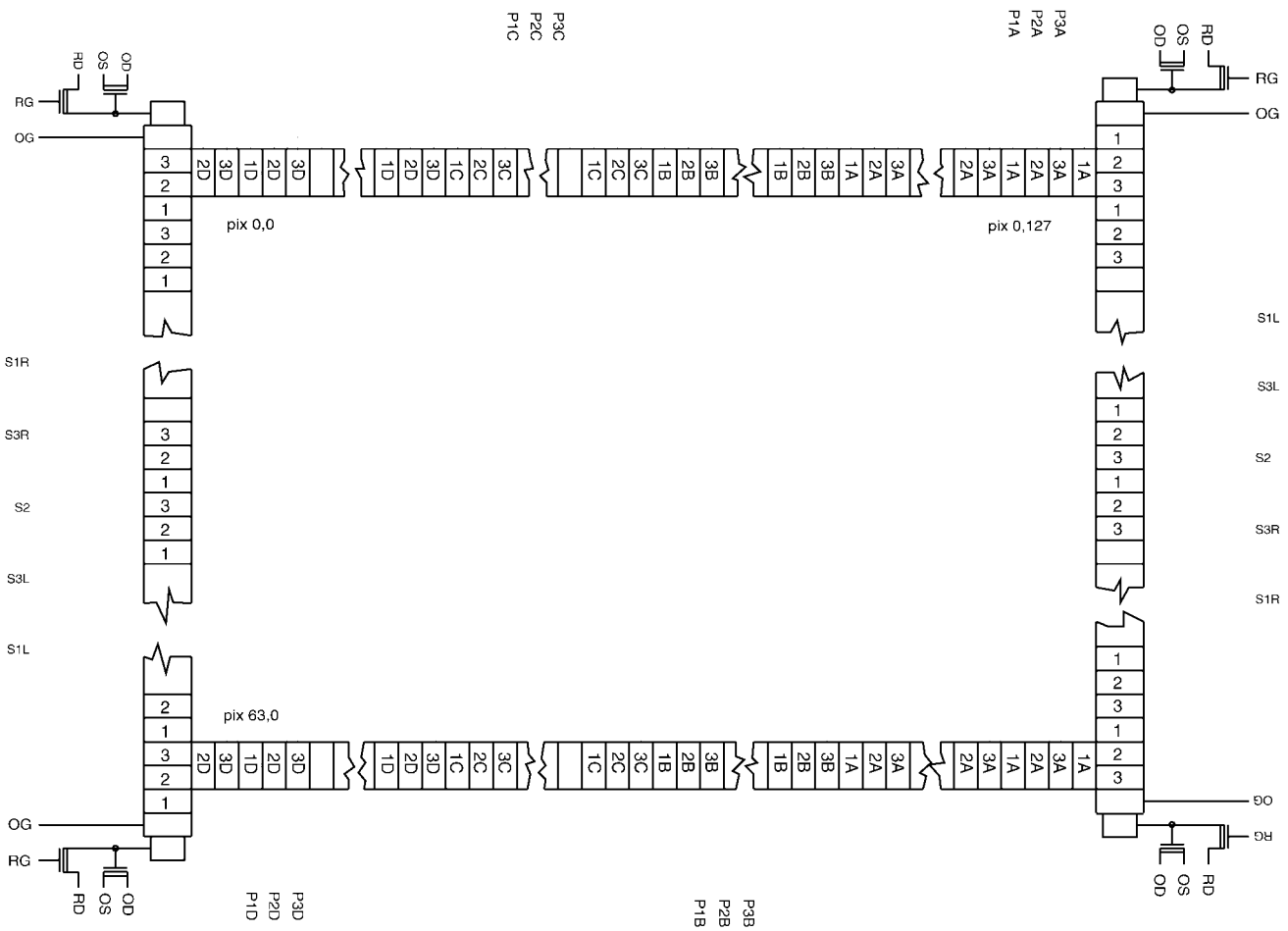

FIG. 3.—Layout of 64 × 128 frame transfer CCD. The device is constructed as four independently clocked sections of 64 × 32 pixels. For frame transfer, the image area parallel clocks (C+D) are wired together, and the storage area parallel clocks (A+B) are wired together. A parallel transfer moves charge rightward on the diagram. Each serial register has two output amplifiers. The CCD is thermoelectrically cooled to reduce the dark current.

of clock cycles (hold time) determines the timing of the clocks to the CCD. As illustrated, each sequence occupies only a few data words.

Normally, for parallel transfers or frame transfer, the serial clocks and dual slope integrator control lines are held in a prespecified state dictated by the CCD architecture. Similarly, the serial transfers require that the parallel clock lines be held in a specified state, possibly a multiphase pinned (MPP) mode as illustrated here. This allows all control lines to be generated simultaneously as one 24 bit word. The assignment of control signals to the 24 bit DSP word is given in Figure 5*b*.

4. CIRCUIT DESCRIPTIONS

Clock drivers convert the logic level signals from the clock generator to the voltage levels required by the CCD. As shown in Figure 6, the circuit topology is based upon a fast analog switch. Prototypes of this circuit indicate that switching times are approximately 100 ns. The rise/fall time of the output is about 50 ns, with propagation delay through the switch accounting for the rest. The analog switch output is either V_H or V_L depending on the input control sequence. Clock drivers are provided for each of the control signals to the CCD, plus a few spares for future use.

The output voltage levels produced by the clock drivers are derived from op-amp voltage buffers. Separate voltage regulators are used for the reset driver, the parallel clock drivers, and the serial clock drivers to avoid crosstalk through the power supply lines. The input to each unity gain buffer amp is an adjustable voltage divider derived from a stable reference. Separate positive and negative references are provided. Similar voltage reference circuits are use to produce the bias levels (RD, OD, OW) required by the CCD.

Two preamplifiers provide voltage gain and buffer the signal to be sent to the dual slope integrators. The circuit topology of each preamplifier is shown in Figure 6. The CCD serial register output field-effect transistor (FET) drives a 15 kΩ re-

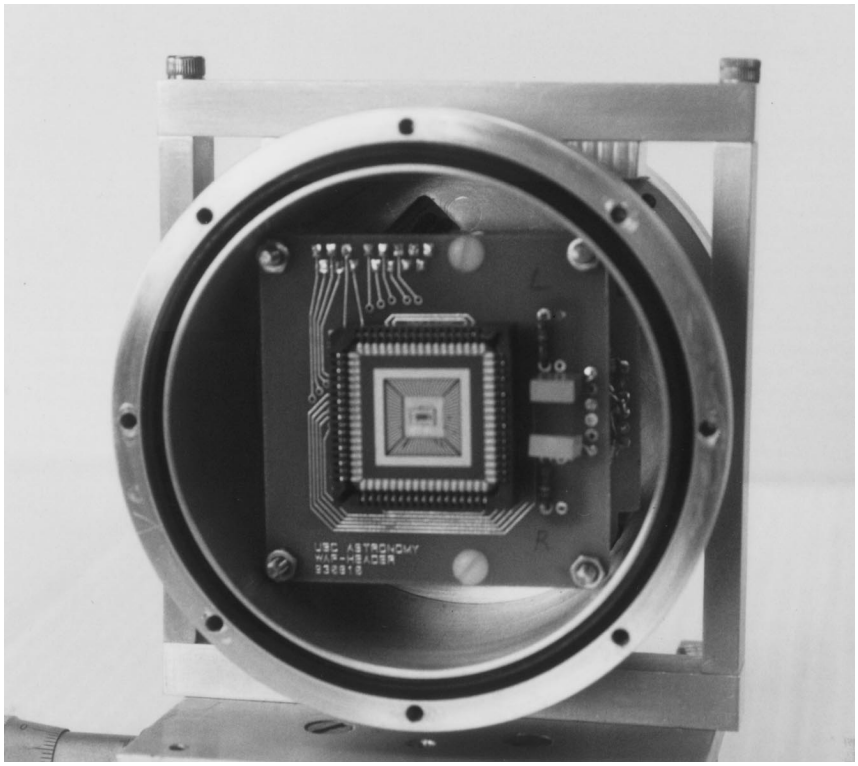

FIG. 4*a*

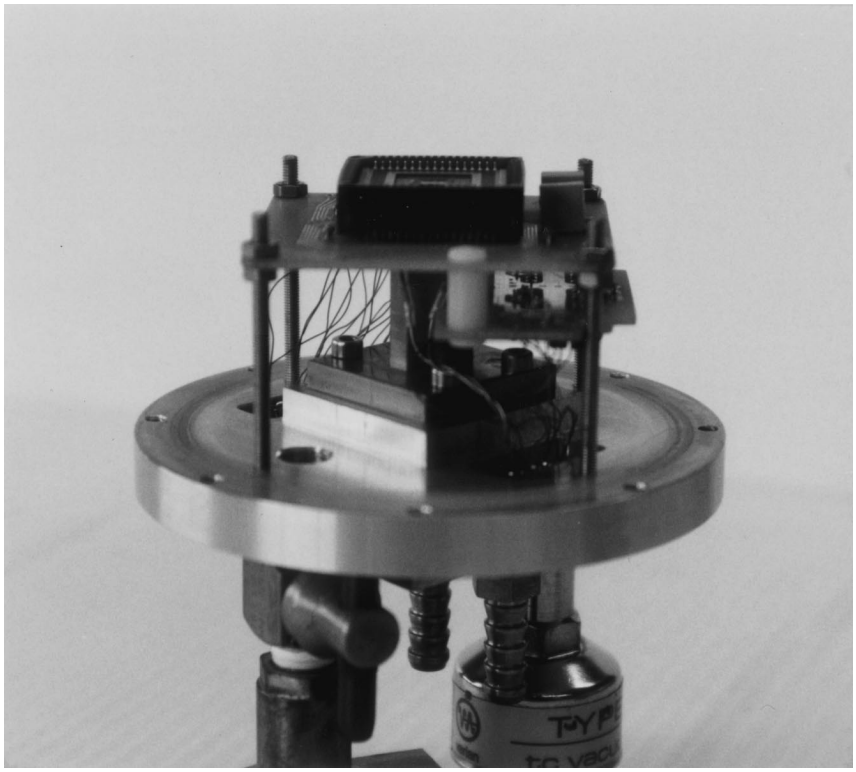

FIG. 4*b*

FIG. 4.—Photographs of the wave front sensor CCD. (*a*) Visible details include the 68 pin CCD package, the circuit board and socket, numerous signal traces, and the O-ring seal for the housing. (*b*) Visible details include the support system for the CCD and preamplifier circuit boards and the heat sink arrangement for the TE cooler directly under the CCD. The mounting allows the housing to rotate.

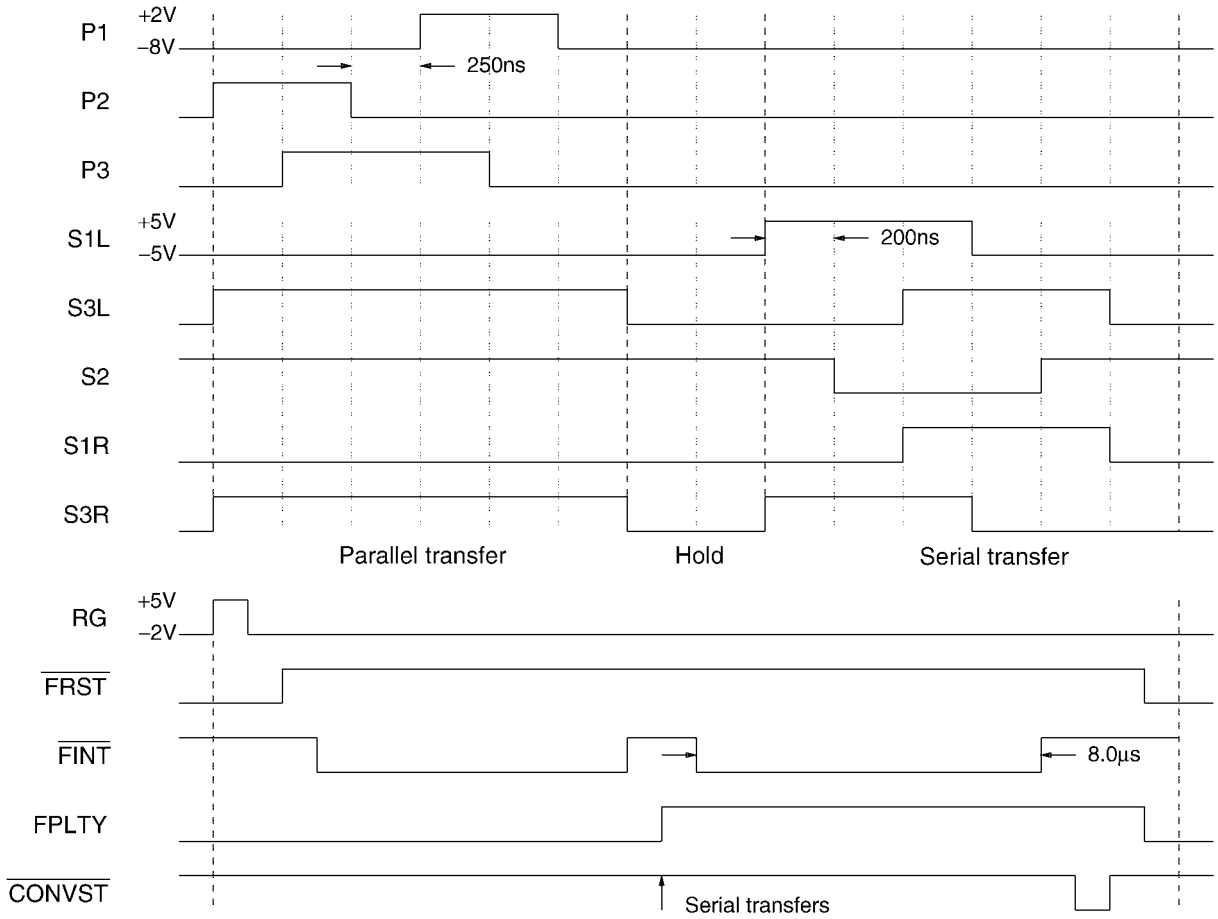

FIG. 5*a*

Bit	Signal	Frame transfer	Parallel readout	Parallel flush	INT+	Serial transfer	INT−	Serial flush
D23	P1AB	000110	000110	000110	00000	000000	00000	000000
D22	P2AB	110000	110000	110000	00000	000000	00000	000000
D21	P3AB	011100	011100	011100	00000	000000	00000	000000
D20	P1CD	000110	000000	000110	00000	000000	00000	000000
D19	P2CD	110000	000000	110000	00000	000000	00000	000000
D18	P3CD	011100	000000	011100	00000	000000	00000	000000
D17	TG	000000	000000	000000	00000	000000	00000	000000
D16	SPARE	000000	000000	000000	00000	000000	00000	000000
D15	S1L	000000	000000	111111	00000	111000	00000	111000
D14	S3L	111110	111110	111111	00000	001110	00000	001110
D13	S2	111111	111111	111111	11111	100011	11111	100011
D12	S1R	000000	000000	111111	00000	001110	00000	001110
D11	S3R	111110	111110	111111	00000	111000	00000	111000
D10	RG	000000	000000	111111	10000	000000	00000	001100
D9	SW	000000	000000	000000	00000	000000	00000	000000
D8	SPARE	000000	000000	000000	00000	000000	00000	000000
D7	$\overline{\text{FRST}}$	000000	000000	000000	01111	111111	11110	000000
D6	$\overline{\text{FINT}}$	111111	111111	111111	11011	111111	01111	111111
D5	FPLTY	000000	000000	000000	00001	111111	11110	000000
D4	$\overline{\text{CONVST}}$	111111	111111	111111	11111	111111	11011	111111
D3	SPARE	000000	000000	000000	00000	000000	00000	000000
D2	SPARE	000000	000000	000000	00000	000000	00000	000000
D1	SPARE	000000	000000	000000	00000	000000	00000	000000
D0	$\overline{\text{BUSY}}$	000001	000001	000001	00001	000001	00001	000001

FIG. 5*b*

FIG. 5.—Sequencing diagram. (*a*) The sequence of signals applied to the CCD parallel clocks, serial clocks, reset transistors, and the control lines for the dual slope integrator. (*b*) The sequence fragments used to generate the clock and control signals. Each bit of the data word corresponds to one of the signals of the sequencing diagram.

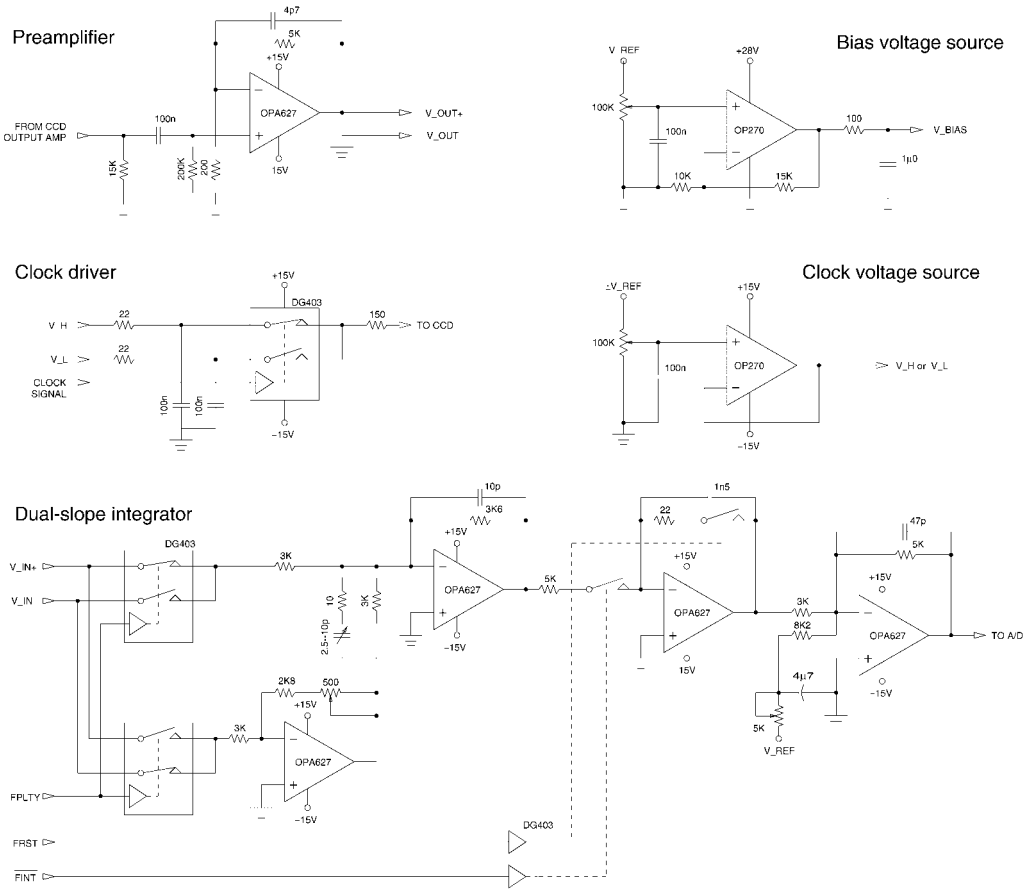

FIG. 6.—Clock driver and signal processing circuits. Op-amp voltage buffers feed an analog switch-based clock driver. The input signal is at CMOS logic levels. The output voltage swings between V_H and V_L, with a typical switching time of about 100 ns. The preamplifier is based on a low-noise OPA627 op-amp and provides a gain of 25. The dual-slope integrator circuit acts as a bandpass filter to suppress the 1/f noise of the CCD output MOSFET amplifier and the reset noise of the CCD.

sistor that is capacitively coupled to a low-noise, wide-bandwidth OPA627 op-amp. Each signal is amplified by a factor of 25 and exits the housing with an associated ground reference.

For the preamplifiers, the input voltage noise density is less than 4.5 nV $Hz^{-1/2}$, while the input current noise density is less than 2.5 fA $Hz^{-1/2}$, as listed in the Burr-Brown data book (Burr-Brown 1994). Since the current noise density is negligible when combined with a 15 kΩ source resistance, a buffer FET to lower the source impedance is unnecessary. With a signal bandwidth of 50 kHz, the preamplifier noise contribution will be 1 μV. By comparison, even for a low CCD read noise of 2.5 e^-, a CCD FET output with a gain of 1.5 μV per e^- will produce thermal noise of 4 μV.

Each preamplifier output and associated ground reference that extracts the CCD signal. As shown in Figure 6, the circuit configuration is that of a differential amplifier with offset adjustment and switchable input polarity, followed by an op-amp integrator. Analog switches configure the input differential signal. The integrator RC time constant is set by a 5 kΩ resistor and 1.5 nF capacitor to match the 8 μs integration times. The integrator storage capacitor is a low-leakage polystyrene type. At the output of the integrator, a buffer op-amp introduces a variable voltage offset and provides a low-impedance source for the analog-to-digital converter. The A/D digital outputs are buffered by four 8 bit registers, so that noise on the DSP data bus does not corrupt the conversion process.

The op-amps of the dual slope integrator signal chain (also OPA627) were chosen for their low noise and fast settling times. These are essential in order to obtain true 16 bit data from the A/D converter. The A/D converter chosen is a monolithic AD7884 chip, calibrated for 16 bit linearity, with an internal sample-and-hold circuit (Analog Devices 1994). The sample and hold tracks the buffer op-amp output during the dual-slope integration and samples the stable signal at the end of the process. The data conversion is pipelined—that is, the A/D conversion is started at the end of each pixel period with the result becoming available during the next pixel period. The conversion time is 5.6 μs, which is more than adequate for the

50 kpixel s^{-1} readout rate (20 μs $pixel^{-1}$) of the controller and allows some future flexibility for speeding up the controller by doubling the pixel rate.

Physically, the preamplifiers are located inside the CCD vacuum housing. The clock drivers and voltage references are located on two small boards only inches away. Two channels of analog signal processing occupy one VME-sized board and are located a few feet away. The digital signal processor, address decoder circuitry, differential line drivers, and serial interface make up a second VME-sized board in the card cage.

Power for the entire wave front sensor is supplied by linear power supplies at +28 V, ±15 V, and +5 V.

5. TIMING AND OPERATION

Software downloaded from the host computer configures the DSP controller to do many standard CCD functions such as (1) frame transfer of the image pixels to the storage array, (2) parallel shift forward or backward, (3) multiple parallel shifts for vertical binning, (4) serial shift and read, (5) multiple serial shifts and read for serial register binning, (6) flush pixel, and (7) multiple flushes for line or array clearing. Readout of the CCD array is accomplished with an ensemble of these building block functions.

The operation of the CCD controller is set up by the host computer, which downloads the program code and sequence fragments into the DSP. Additional data loaded into the DSP specify the size of the array, the parallel and serial binning, and the sequence of operations. For each operation, the DSP accesses the sequence fragment and steps through it using the associated timing information. Elementary operations such as a single pixel read or a parallel shift are repeated to read an entire line or to perform a frame transfer. The DSP executes the specified operations on a frame-by-frame basis and can return data to the host computer via a fast SBus serial interface at up to 10 Mbits s^{-1}.

With the appropriate sequence fragments, the CCD can be read out through one or both output amplifiers at either end of the serial register as 64 × 64 (with frame transfer) or as 64 × 128 pixels. By specifying the hold time for each data word, the host software configures the parallel and serial clock rates and the overall frame rate. The versatility of the controller allows the CCD to be read pixel by pixel or using the curvature sensing subaperture patterns, with programmable binning, clock rates, frame transfer, and multiple output amplifiers. For operation as a curvature sensor, an additional list detailing the sequence of operations to read the array into subapertures is downloaded into the DSP. The superpixel list details the parallel transfers, the serial register binning per superpixel, and the subaperture to which each superpixel belongs. Each image from the sensor involves processing the list one time. For the 19 element sensor pattern of Figure 2, the list has 104 elements.

For the small-frame transfer CCD, the elementary sequencing operations are shown in Figure 5. The timing is set so that the serial transfers occur in between the integration periods of the dual slope integrator, since there is no on-chip summing well. Normal operation of the CCD involves a readout rate of 20 μs $pixel^{-1}$, with dual-slope integration times of 8 μs. A single three-phase parallel transfer requires 2.5 μs, while a single serial transfer takes 1.2 μs. Readout involves both output amplifiers from the serial register on the storage side of the array. For a 16 × 16 image, the readout time is approximately 2.5 ms. For the 19 subaperture mode, the readout time is 2.0 ms. The device can be read out at a rate approaching 500 frames s^{-1}. If necessary, the readout could be timed for 10 μs $pixel^{-1}$, which effectively doubles the frame rate.

The fastest clock sequencing is required during frame transfer. Note that this is a very repetitive operation, generated by stepping through a few sequence fragments in a "DO" loop. The limitation on clock rate is the clock driver propagation delay and rise/fall time. On the CCD, the rate of parallel transfer clocking is limited by the capacitance per pixel and the number of pixels per row. Since the array is only 64 × 64 pixels, fast transfer with parallel clock phases of 250 ns is feasible (frame transfer in less than 100 μs). With an integration time of 5 ms and frame transfer time of 100 μs, the resulting on-target duty cycle is about 98%. Streaking during frame transfer (with no shutter) is kept to a minimum.

6. EXTRACTING THE CURVATURE SIGNAL

The CCD curvature sensor operates by sampling the defocused guide star image into an annular pattern of subapertures. Sample patterns are shown in Figure 2 for a 32 × 32 grid. The dashed circle represents the outline of the spot produced by the defocused beam. The illuminated area of each subaperture is roughly equal to minimize the variation in signal-to-noise ratio over the pattern. Normally the center spot of the pattern is partially covered by the shadow of the telescope secondary mirror. The number of subapertures and the subaperture design are set by the scale of the atmospheric seeing relative to the telescope aperture, the order of correction of the adaptive optics system, and the pattern of actuators of the deformable mirror.

Since the annular patterns of the subapertures do not fit exactly onto the grid of the CCD, some spatial quantization error will result. Comparing the area of the summed pixels to the area of each subaperture, a first-order estimate of the spatial quantization error on a 32 × 32 grid is approximately 3%. Sampling on a coarser grid introduces an error that is several times larger, while a finer grid involves many more pixels that would compromise the sensor frame rate.

After the image is acquired, the DSP processes the subaperture data to extract the curvature signal. The subapertures have different responsivity, bias level, and dark current according to the number of pixels in each, which must be compensated before the curvature signal is computed. Flat-fielding involves only a deterministic scale factor to compensate for the different subaperture areas and the different gains of the two

output amplifiers. With the large number of pixels of the 64 × 64 array making up each subaperture, the individual pixel-to-pixel variations are largely averaged out. A dark frame is acquired at the beginning of the session using the subaperture readout mode to compensate for the differing bias levels and dark counts. When required, the dark frame can be reacquired to account for temperature changes or drift in the CCD or signal processing gain.

For each subaperture, the curvature signal is determined from the formula

$$\frac{\Delta I}{I} = \frac{G(I - I_B) - I_S}{I_S}, \quad (1)$$

where I is the subaperture data, I_B is the subaperture dark signal, $I_S = \Sigma(I - I_B)$ is the bias-corrected sum of the subapertures from the bias and image frames, and G is a geometric scaling factor.

To minimize the number of divide operations, which consume many processor cycles, each subaperture signal is scaled so that all the curvature calculations use the same normalization factor. The scaling factor is based on the illuminated area (and output amplifier gain) and gives the equivalent signal for the full aperture. For example, a subaperture with 1/20th of the total area would be scaled by a factor of 20. This approach avoids calculating a different normalization factor for each subaperture.

After each integration, readout of the CCD gives the raw subaperture signals. For each signal, the bias level is subtracted, and the result is scaled by the geometric factor G. The subaperture sum I_S and the normalization factor I_S^{-1} are computed. Finally, the curvature signal per subaperture is calculated as per equation (1). Once the CCD readout is complete, the processor takes less than 20 μs to derive curvatures for all subapertures.

7. SUMMARY

Overall, the prototype has illustrated that a CCD wave front curvature sensor is a practical, technically viable device. The current version is capable of 500 frames s^{-1}, with less than 10 e^- read noise. A small-format, low-noise, high quantum efficiency, frame transfer CCD with a DSP-based controller would make a near-ideal versatile wave front sensor.

In operation, superpixel binning during the sensor readout makes fast frame rates and low-noise readout compatible. The curvature signal can be extracted efficiently and quickly, without extensive flat-fielding. Such a small sensor is readily cooled. The controller is flexible and could work with many other CCD detectors, with or without frame transfer, with minimal hardware or software modifications.

The DSP-based design for the CCD controller means that the code for the entire system is highly compact and efficient. The clock sequences are directly generated from a minimum of sequence fragments. Clock timing is done with software. The sequence fragments are only a few words long and are easily generated by hand.

Without extrapolating the technology too far, one can envision a versatile wave front sensor with a broadband quantum efficiency of 80%, a read noise of 2 e^-, split parallel and serial registers, and four output amplifiers operating at 100 kpixel s^{-1} to provide a sampling rate of 2000 frames s^{-1}. In MPP mode, the cooled device would have negligible dark current for short exposures. Newer 80 MHz versions of the DSP56002 would permit the timing resolution and serial link data rate to be doubled. Such a wave front sensor could be pocket sized.

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