

FEATURES

- Full 132 Mbytes/sec Transfer Rate
- PCI Bus Operation to 33 MHz
- PCI Proposed 2.2 Compliant Target/Slave
- Add-On Bus up to 40 MHz
- Programmable Prefetch and Wait States
- 8/16/32 Bit Add-On Bus
- Four Definable Pass-Thru Regions
- Two 32 Byte Burstable FIFOs
- Active/Passive Add-On Bus Operation
- Mailbox Registers with Byte Level Status
- Direct Mail Box Data Strobe/Int Pin
- Mailbox Read/Write Interrupts
- Direct PCI and Add-On Interrupt Pins
- Plug-n-Play Compatible
- Two wire Serial Bus nvRAM Support
- Optional External BIOS
- 160-pin PQFP

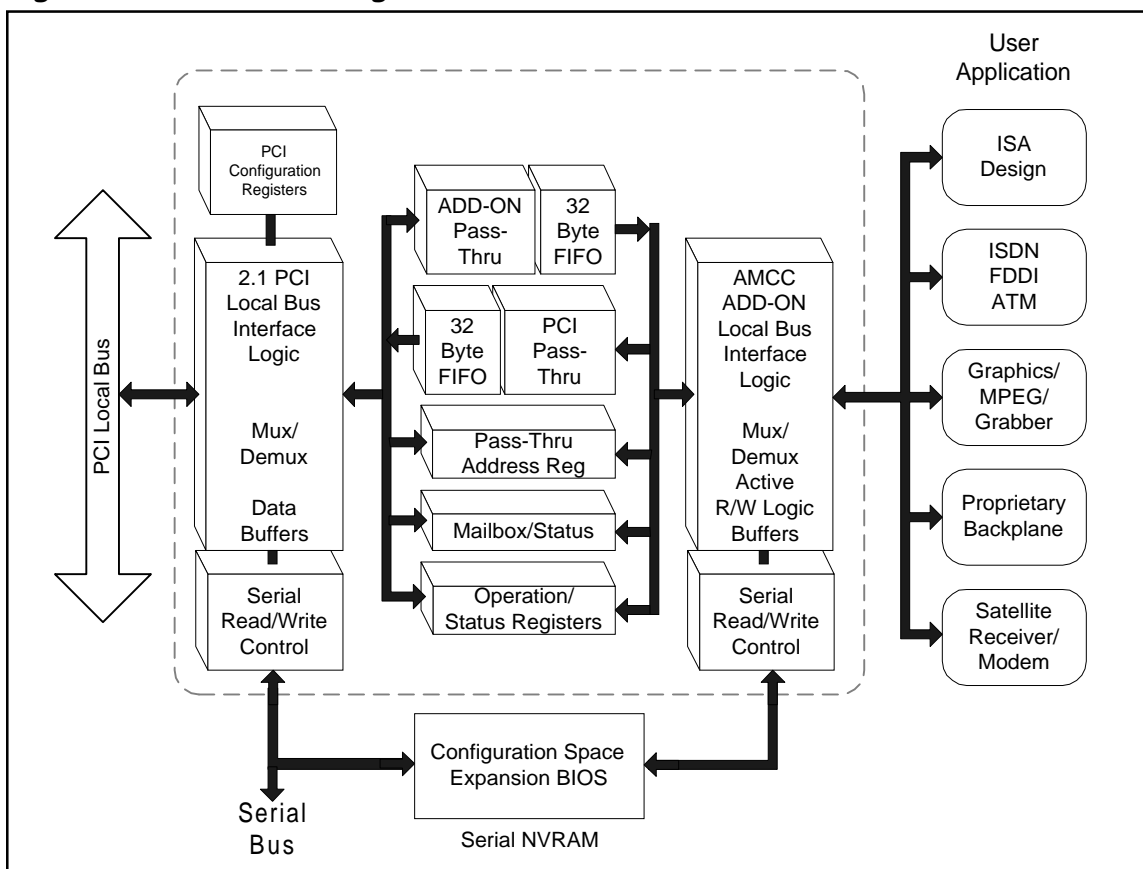
INTRODUCTION

The AMCC S5920 was developed to provide the designer with a single multifunction device offering a flexible and easy way to connect to the PCI Bus. By using the S5920, the designer eliminates the task of assuring PCI bus compliance and the necessity to understand PCI Bus timing requirements when interfacing a new application.

The complex PCI bus signals are converted through the S5920 into an easy-to-use 8/16/32 bit user bus referred to as the user Add-On Bus. The Add-On Bus allows user designs to operate async or sync operation up to 40 MHz.

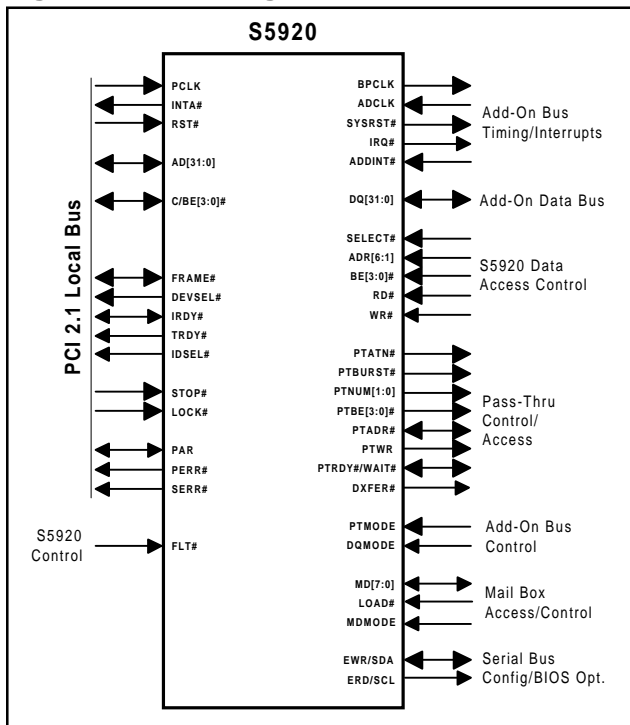
Since the S5920 is a PCI Target/Slave device only, it's cost is significantly less than PCI Bus Master solutions. The S5920 is PCI Purposed 2.2 compliant and can support data transfer rates up to 132 Mbytes/sec. Burst transfers and single data transfers are both supported. Figure 1 shows the block diagram for the S5920. Figure 2 shows basic S5920 signal connections.

Figure 1. S5920 Block Diagram



Many additional S5920 features offer the user easier hardware and software implementation. Up to four memory or I/O size definable blocks, referred to as Pass-Thru regions, are provided for multiple device configurations. Data transfers via a Pass-Thru region can be performed either direct to the Add-On bus or through two 32 byte burstable FIFOs. Added read prefetch and programmable FIFO wait state features allow the user to tune system performance. The Pass-Thru data channel also supports an active/passive mode bus interface. Passive mode requires the designer to transfer data by externally driving the Add-On Bus. Active mode minimizes design components by enabling internal logic to drive or acquire the Add-On Bus to read or write data independently. Active mode provides programmable wait state generation for slower Add-On designs.

Figure 2. S5920 Signals



Two 32 bit mailbox registers are implemented for additional data or user defined status/command transfers. Each mailbox may be examined for empty or full, at the byte level, through a mailbox status register. Mailbox transfers can be either register style or hardware direct. Dedicated external mailbox data and strobe pins are provided for direct hardware read/writes and allow Add-On to PCI interrupt capabilities. A direct Add-On to PCI bus interrupt pin is incorporated adding design flexibility.

The S5920 supports a two wire serial nvRAM. This allows the designer to customize the device configuration to be loaded during power-up initialization. An expansion BIOS may also be contained in the nvRAM.

S5920 REGISTER ARCHITECTURE

S5920 communications, control and configuration is performed through three primary groups of registers: PCI Configuration Registers, PCI Operation Registers and Add-On Operation Registers. All of these registers are user configurable through their associated buses and from the external nvRAM. The following sections provide a brief overview of each register group and the nvRAM interface.

PCI Configuration Registers

All PCI compliant devices are required to provide a group of PCI configuration registers. These registers are polled by the host BIOS system during power-up initialization. They contain specific device and product information such as Vendor ID, Device ID, Subsystem Vendor ID, memory requirements, etc. These registers are located in the S5920 and are either initialized with predefined default values or user customized definitions contained in the external nvRAM.

PCI Bus Accessible Stuff

The second group of registers are the PCI Operation Registers. This group of registers is accessible to the PCI Bus. These are the primary registers through which the PCI Host configures the S5920 operation and communicates with the Add-On Bus. These registers encompass the PCI bus mailboxes, Pass-Thru/FIFO data channel and Status/ Control registers.

Add-On Bus Accessible Registers

The last register group consists of the Add-On Operation Registers. This group of registers is accessible via the Add-On Bus. These are the primary registers through which the Add-On application configures S5920 operation and communicates with the PCI Bus. These registers encompass the Add-On bus mailboxes, Pass-Thru/FIFO Registers and Status/Control Registers.

SERIAL NON-VOLATILE INTERFACE

Previously indicated, the S5920 contains the required set of PCI Configuration Registers. These registers can be initialized with default values or with customized values contained in an external nvRAM. The nvRAM allows the Add-On card manufacturer to initialize the S5920 with his specific Vendor ID values along with other desired S5920 operation characteristics.

MAILBOX OPERATION

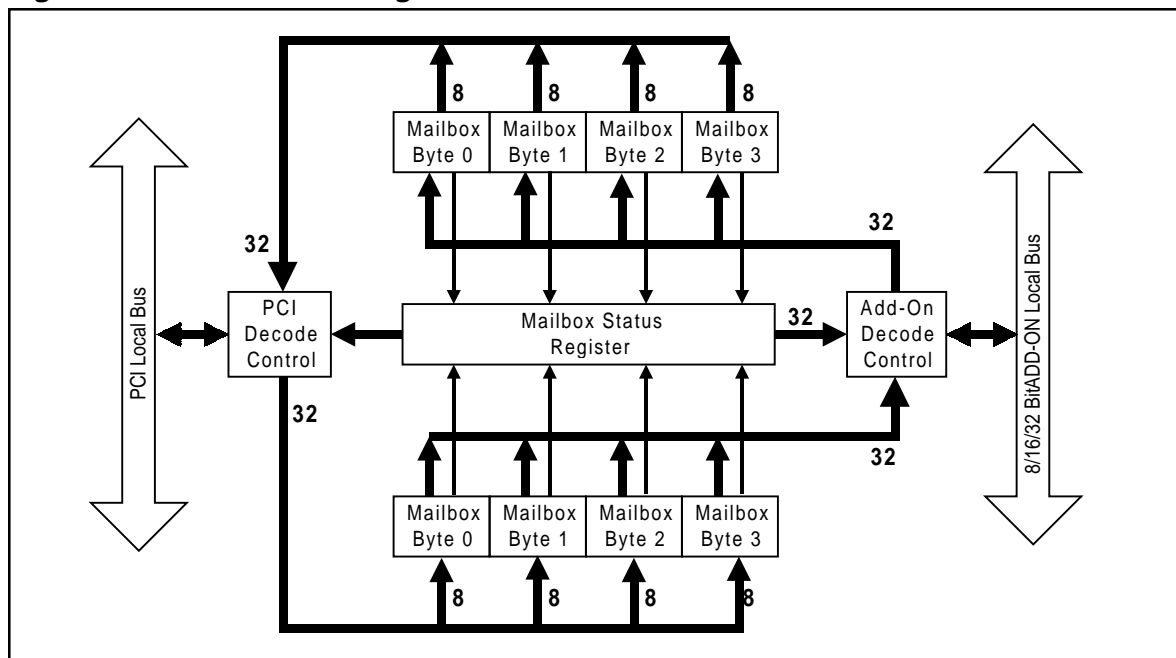
The mailbox registers are divided into two 4 byte sets. Each set is dedicated to one bus for data transfer to the other bus. Figure 3 shows a block diagram of the mailbox section of the S5920. The provision of mailbox registers provides data or user defined command/status transfer capability between two busses. An empty/full indication for each mailbox register, at the byte level, is determined by polling a status register accessible to both the PCI and Add-On busses. Providing mailbox byte level full indications allows greater flexibility in 8, 16 or 32 bit designs; i.e. transferring a single byte in 8 bit Add-On bus without requiring the assembly or disassembly of 32 bit data.

A mailbox byte level interrupt feature for PCI or Add-On busses is provided. Bit locations configured within the S5920 operation registers can select which mailbox byte is to generate an interrupt when the mailbox is written to. Interrupts can be generated to the PCI or Add-On busses. PCI Bus interrupts may also be generated from direct hardware interfacing due to a unique S5920 feature. The Add-On mailbox is hardware accessible via a set of dedicated device pins. A single load pulse latches data into the mailbox generating an interrupt, if enabled.

PASS-THRU OPERATION

Pass-Thru region accesses can execute PCI bus cycles in real time or through an internal FIFO. Real time operation allows the PCI bus to directly read or write to Add-On Bus resources. The S5920 allows the designer to declare up to four individual Pass-Thru regions. Each region may be defined as 8, 16 or 32 bits wide, mapped into memory or I/O system space and may be up to 512 MB in size. Figure 4 shows a basic block diagram of the S5920 Pass-Thru architecture.

Figure 3. Mailbox Block Diagram



Host communications to the Pass-Thru data channel utilizes dedicated Add-On Bus pins to signal that a PCI read or write has been requested. User logic decodes these signals to determine if it must read or write data to the S5920 to satisfy the PCI request. Information decoded includes: PCI read/write transaction request, the byte lanes involved, the specific Pass-Thru region accessed and the request is a burst or single cycle access.

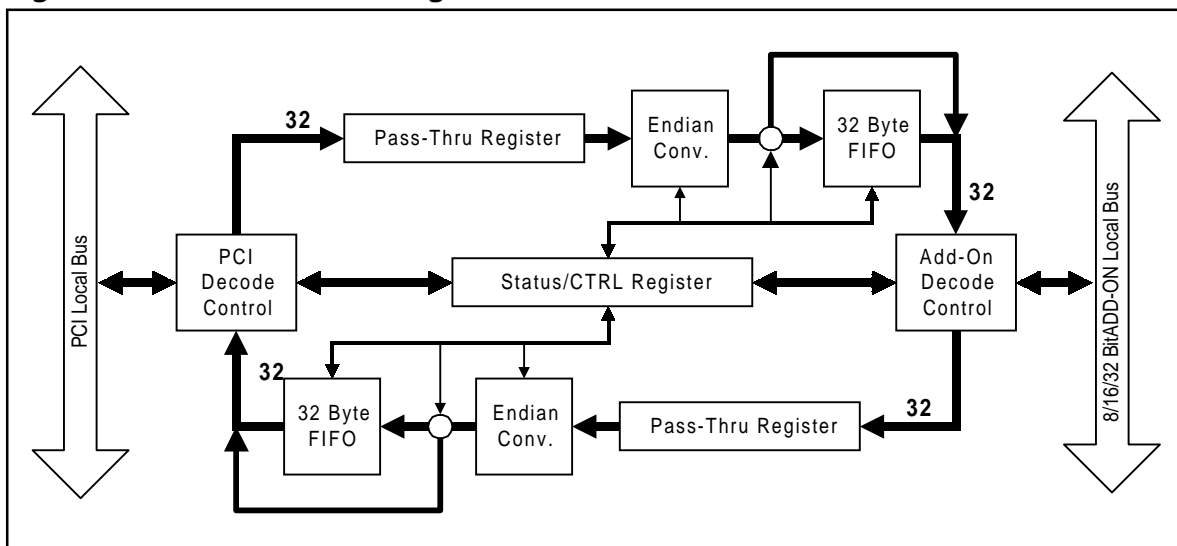
Pass-Thru operation supports single PCI data cycles and PCI data bursts. During PCI burst operations, the S5920 is capable of transferring data at the full PCI bandwidth. Should slower Add-On logic be implemented, the S5920 will issue a PCI bus retry until the requested transfer is completed.

To increase data throughput, the Pass-Thru channel incorporates two 32 byte FIFOs. One FIFO is dedicated to PCI read data while the other is dedicated to PCI write data. Enabling the write FIFO allows the S5920 to accept zero wait state bursts from the PCI bus regardless of the Add-On bus application design speed.

Enabling the read FIFO allows data to be optionally prefetched from the Add-On Bus. This can greatly improve performance of slow Add-On bus designs. PCI read cycles can be performed with zero wait states since data has been prefetched into the FIFO. Either of the write/read FIFOs can be disabled or enabled to tune system performance.

The Add-On bus can be operated in two different modes: active or passive. The passive mode of operation mimics that of the S5933 Add-On bus operation. The user design drives S5920 pins to read or write data. In active mode, the Add-On Bus is driven from an S5920 internal state machine. This reduces component count in cost sensitive designs. Active mode also incorporates programmable wait states from 0 to 7.

Figure 4. Pass-Thru Block Diagram



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