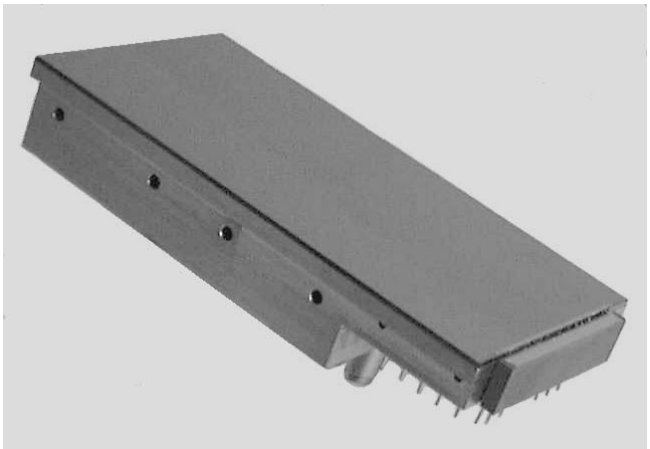
e2v technologies

CCD44-82 Back Illuminated High Performance CCD Sensor

FEATURES

- 2048 by 4096 Pixel Format
- 15.0 μm Square Pixels
- Image Area 30.7 x 61.4 mm
- Back Illuminated Format for High Quantum Efficiency
- Low Noise Output Amplifiers
- Wide Dynamic Range
- Symmetrical Anti-static Gate Protection
- 3-side Buttable Package
- Gated Dump Drain on Readout Register
- Flatness better than 20 μm peak to valley



APPLICATIONS

- Astronomy
- Scientific Imaging

INTRODUCTION

This version of the CCD44 family of CCD sensors has full-frame architecture. Back illumination technology, in combination with an extremely low noise amplifier, makes the device well suited to the most demanding applications, such as astronomy.

The output amplifier is designed to give excellent noise levels at low pixel rates and can match the noise performance of most conventional scientific CCDs at pixel rates as high as 1 MHz. The low output impedance and optional FET buffer simplify the interface with external electronics.

The readout register has a gate controlled dump-drain to allow fast dumping of unwanted data. The register is designed to accommodate three image pixels of charge and a summing well is provided capable of holding four image pixels. The output amplifier has a feature to enable the responsivity to be reduced, allowing the reading of such large charge packets.

The device is supplied in a package designed to facilitate the construction of large close-butted mosaics and is designed to be used cryogenically. The design of the package will ensure that the device flatness is maintained at the working temperature.

The sensor is shipped in a protective container, but no permanent window is fitted.

TYPICAL PERFORMANCE (at 173 K)

Pixel readout frequency	20 - 1000	kHz
Output amplifier sensitivity	6.0	$\mu V/e^-$
Peak signal	200	ke^-/pixel
Spectral range	200 - 1060	nm
Readout noise (at 20 kHz)	2.5	e^- rms
QE at 500 nm	90	%
Charge transfer efficiency	99.9995	%

GENERAL DATA

Format

Image area	30.7 x 61.4	mm
Active pixels (H)	2048	
(V)	4096 + 6	
Pixel size	15 x 15	μm
Number of output amplifiers	2	
Number of underscan (serial) pixels	50	

The device has a 100% fill factor.

Package

Format	invar metal package with PGA connector	
Focal plane height above base	14.0	mm
Package size	31.7 x 66.6	mm
Package weight	150	g approx
Number of pins	40	
Inactive edge spacing:		
sides	500 ± 50	μm
top	160 ± 50	μm
bottom (edge connections)	5.0	mm

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PERFORMANCE (at 173 K unless stated)

	Min	Typical	Max	
Peak charge storage (see note 1)	150k	200k	-	e^-/pixel
Peak output voltage (unbinned)		1200		mV
Dark signal at 153 K (see note 2)		0.01	1	e^-/pixel/hour
Charge transfer efficiency (see note 3):				
parallel	99.999	99.9995		%
serial	99.999	99.9998		%
Output amplifier sensitivity (see note 4):				
mode 1	4.5	6.0	-	$\mu V/e^-$
mode 2	-	1.5	-	$\mu V/e^-$
Readout noise at 188 K (see note 5)	-	2.5	4	rms e^-/pixel
Readout frequency (see note 6)	-	20	1000	kHz
Output node capacity (see note 4):				
OG2 low (mode 1)	-	300k	-	electrons
OG2 high (mode 2)	-	1200k	-	electrons
Register capacity	-	600k	-	e^-/pixel

Spectral Response at 173 K (Astronomy broadband devices)

Wavelength (nm)	Spectral Response (QE)		Response Non-uniformity, max (1σ)	
	Typical	Min		
350	50	40	-	%
400	80	70	3	%
500	90	80	-	%
650	80	75	3	%
900	30	25	5	%

Note Devices with alternate spectral response are also available.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level)

	Min	Typical	Max	
I∅/I∅ interphase	-	30	-	nF
I∅/SS	-	60	-	nF
Output impedance	-	350	-	Ω

NOTES

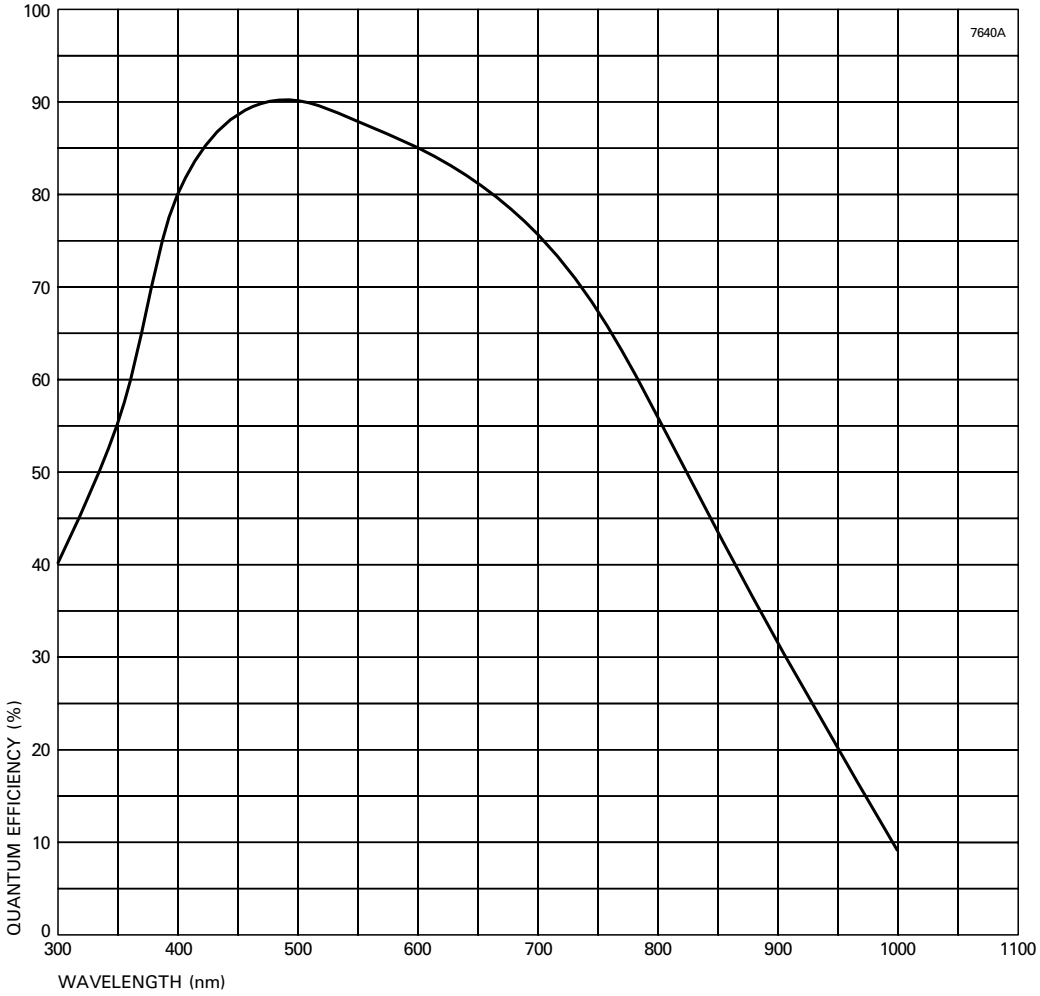
1. Signal level at which resolution begins to degrade.
2. Dark signal is typically measured at 188 K and V_{ss} = +9 V. The dark signal at other temperatures may be estimated from:

   $$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

   where Q_{d0} is the dark current at 293 K.
3. Measurements made using charge generated by X-ray photons of known energy. Charge transfer efficiency is measured for a complete three-phase triplet.
4. Operation of the OG2 gate modifies the output node. OG2 = LO (mode 1) is normally used for low noise, high responsivity. See also note 9.
5. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 10 μs integration period with OG2 = OG1 + 1 V.
6. Readout above 1000 kHz can be achieved but performance to the parameters given cannot be guaranteed.

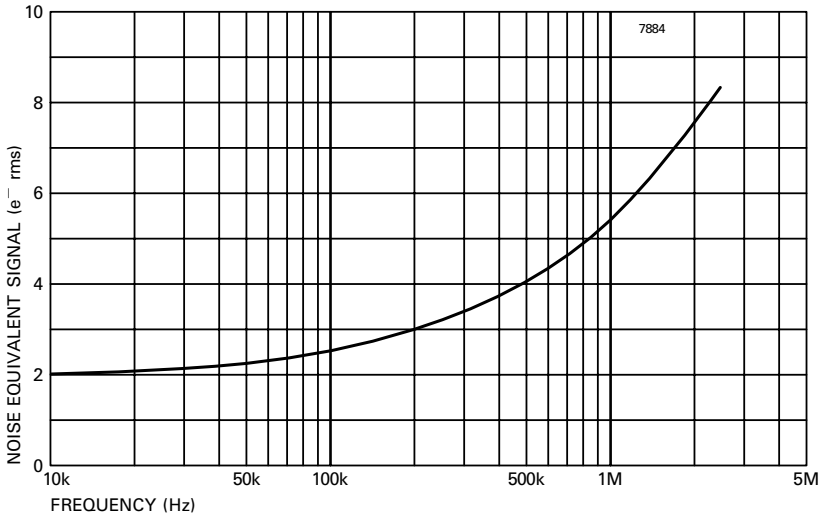
TYPICAL SPECTRAL RESPONSE

(At −90 °C, measured with astronomy broadband AR coating)



TYPICAL OUTPUT CIRCUIT NOISE

(Measured using clamp and sample, temperature range 140 - 230 K)



BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 173 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots Are counted when they have a responsivity of less than 80% of the local mean signal.

White spots Are counted when they have a generation rate equivalent to 100 electrons per pixel per hour at 153 K (typically measured at 188 K). The typical temperature dependence of white spot blemishes is the same as that of the average dark signal, i.e.:

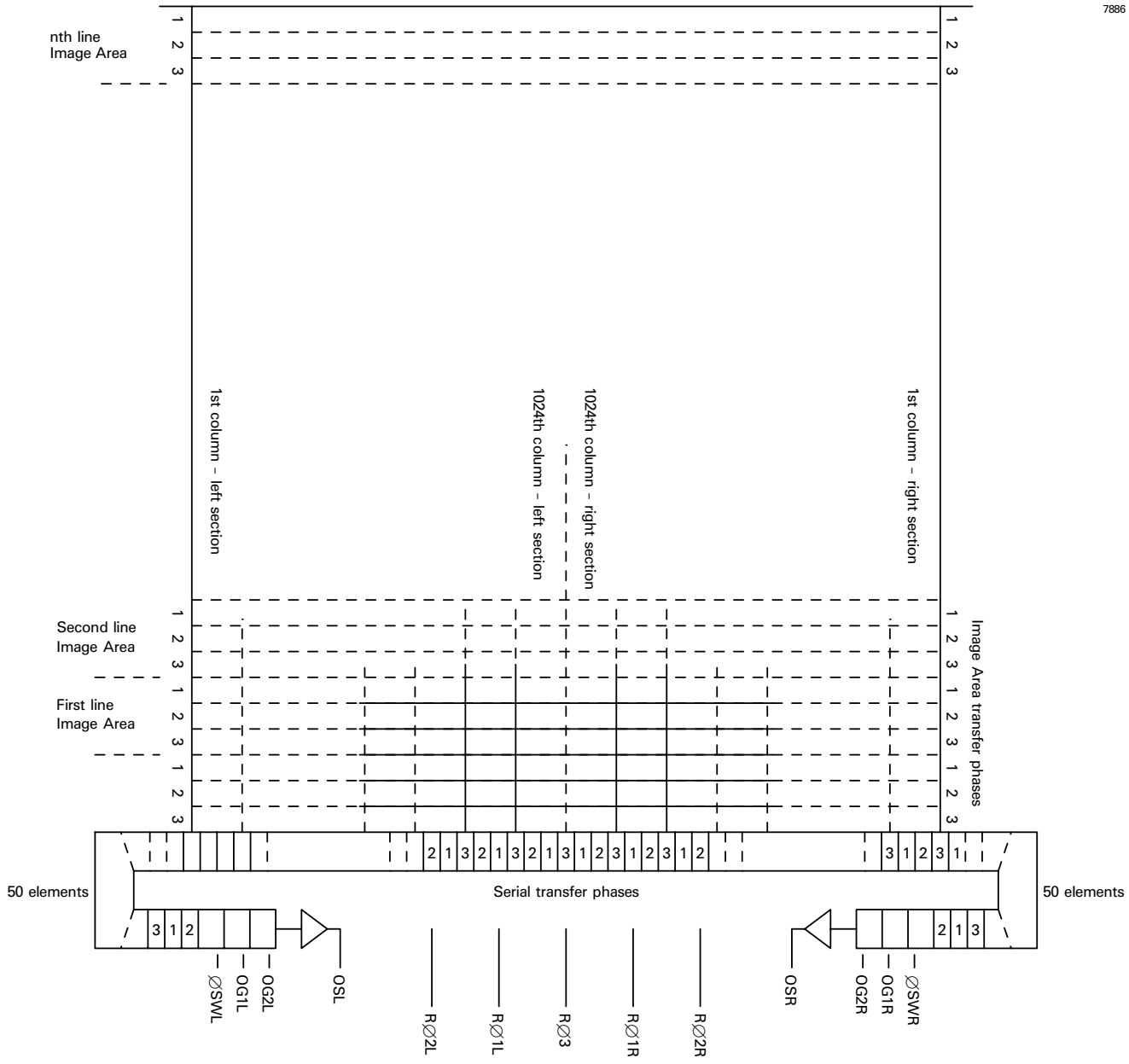
$$Q_d / Q_{d0} = 122T^3 e^{-6400/T}$$

Column defects A column which contains at least 100 white or black defects.

GRADE	0	1	2	3
Column defects (black or white)	2	6	12	24
White spots	250	500	1000	1500
Traps	20	30	50	75
Total spots (black and white)	750	1250	2000	3000

GRADE 5 Devices which are fully functional, with image quality below that of grade 3, and which may not meet all other performance parameters; not all parameters may be tested.

CLOCK ARCHITECTURE



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

40-pin PGA connector

PGA PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 7)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
A1, A8, C1, C8, F2, F7	V_{SS}	Substrate	-	9	-	-
D8	I∅1	Image area clock, phase 1	8	10	14	±20 V
E8	I∅2	Image area clock, phase 2	8	10	14	±20 V
F8	I∅3	Image area clock, phase 3	8	10	14	±20 V
D4	R∅1(L)	Register clock phase 1 (left)	9	11	15	±20 V
E4	R∅2(L)	Register clock phase 2 (left)	9	11	15	±20 V
D5	R∅1(R)	Register clock phase 1 (right)	9	11	15	±20 V
E5	R∅2(R)	Register clock phase 2 (right)	9	11	15	±20 V
F6	R∅3	Register clock phase 3	9	11	15	±20 V
E3	∅R(L)	Reset gate (left)	9	12	15	±20 V
E6	∅R(R)	Reset gate (right)	9	12	15	±20 V
E2	∅SW(L)	Summing well gate (left)	9	11	15	±20 V
E7	∅SW(R)	Summing well gate (right)	9	11	15	±20 V
F3	DG	Dump gate (see note 8)	−0.5	0	15	±20 V
D3	OG1(L)	Output gate 1 (left)	1	3	4	±20 V
D6	OG1(R)	Output gate 1 (right)	1	3	4	±20 V
B2	DD(L)	Dump drain (left)	22	24	26	−0.3 to +30 V
B7	DD(R)	Dump drain (right)	22	24	26	−0.3 to +30 V
D2	OG2(L)	Output gate 2 (left)	see note 9			±20 V
D7	OG2(R)	Output gate 2 (right)	see note 9			±20 V
B1	OD(L)	Output drain (left)	27	29	-	−0.3 to +35 V
B8	OD(R)	Output drain (right)	27	29	-	−0.3 to +35 V
A2	OS(L)	Output source (left)	see note 10			−0.3 to +25 V
A7	OS(R)	Output source (right)	see note 10			−0.3 to +25 V
C2	RD(L)	Reset drain (left)	15	17	-	−0.3 to +25 V
C7	RD(R)	Reset drain (right)	15	17	-	−0.3 to +25 V
Optional connections for 309 JFET						
A3	RL(L)	Load resistor (left)	A_{GND} (0 V)			
A6	RL(R)	Load resistor (right)	A_{GND} (0 V)			
B3	OP(L)	JFET source (left)	see note 11			
B6	OP(R)	JFET source (right)	see note 11			
C3	JD(L)	JFET drain (left)	OD(L) +2 V			
C6	JD(R)	JFET drain (right)	OD(L) +2 V			
Other connections						
D1, F1	Temp	Temperature sensor*	PT100			
E1	-	No connection				

If all voltages are set to the typical values operation at, or close to, specification should be obtained. Some adjustment within the minimum - maximum range specified may be required to optimise performance. Refer to the specific device test data if possible.

Maximum voltage between pairs of pins: OS to OD ±15 V.

Maximum current through any source or drain pin: 10 mA.

The CCD is not electrically connected to the metal package.

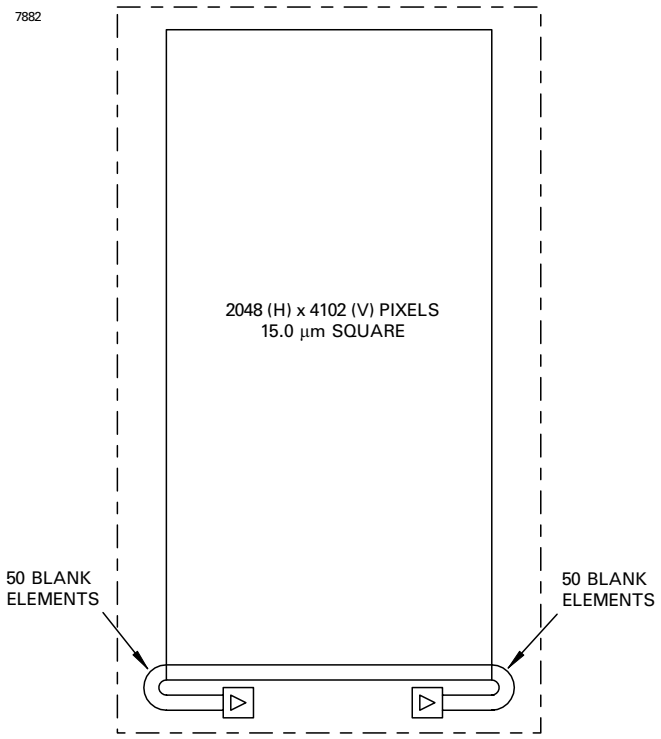
* Full-frame versions only.

NOTES

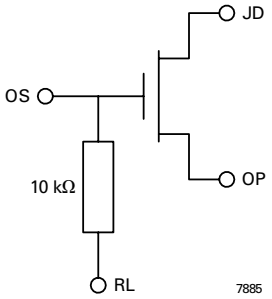
7. Clock pulse low levels 0 ± 0.5 V for image, reset and SW clocks; except RØ low = +1 V (register). For clock signals, the table indicates high levels for clocks.

   With the RØ connections shown, this device will operate through both outputs simultaneously (split serial mode). To operate from the left-hand output only, RØ1(R) and RØ2(R) should be reversed, i.e. pin D5 = RØ2(R) and E5 = RØ1(R).
8. Non-charge dumping level is shown. For charge dumping, DG should be pulsed to 12 ± 2 V.
9. OG2 = OG1 + 1 V; for operation in high responsivity, low noise mode, OG2 should be set to +4 V typical. For operation in low responsivity, increased charge handling mode, OG2 should be set to +20 V.
10. OS = 3 to 5 V below OD typically. Use a 3 - 5 mA current source or a 5 - 10 kΩ load.
11. The JFET is floating, with its gate connected to OS. A floating 10 kΩ load resistor is also connected to OS. The FET may be used to buffer the chip output (OS) if desired; in this case, connect the FET output to A_{GND} via a 5 mA load and RL directly to A_{GND}. (U309 data: V_{GD} and V_{GS} absolute maximum = −25 V). See detail below.

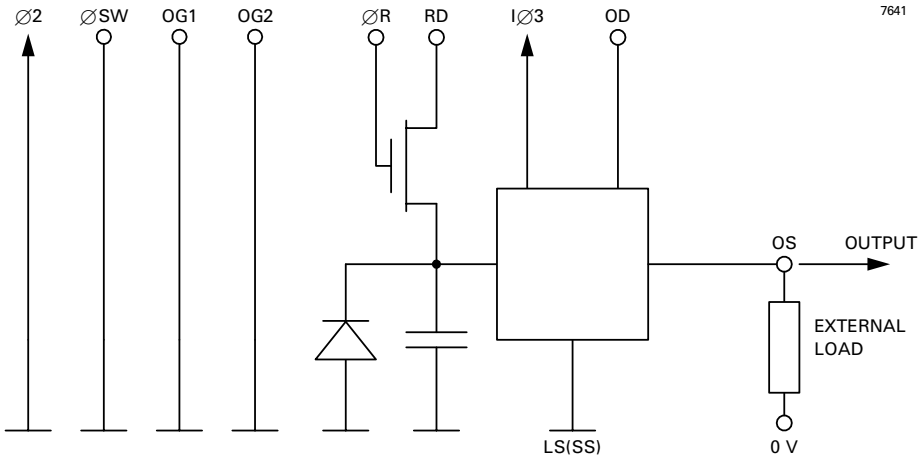
DEVICE SCHEMATIC



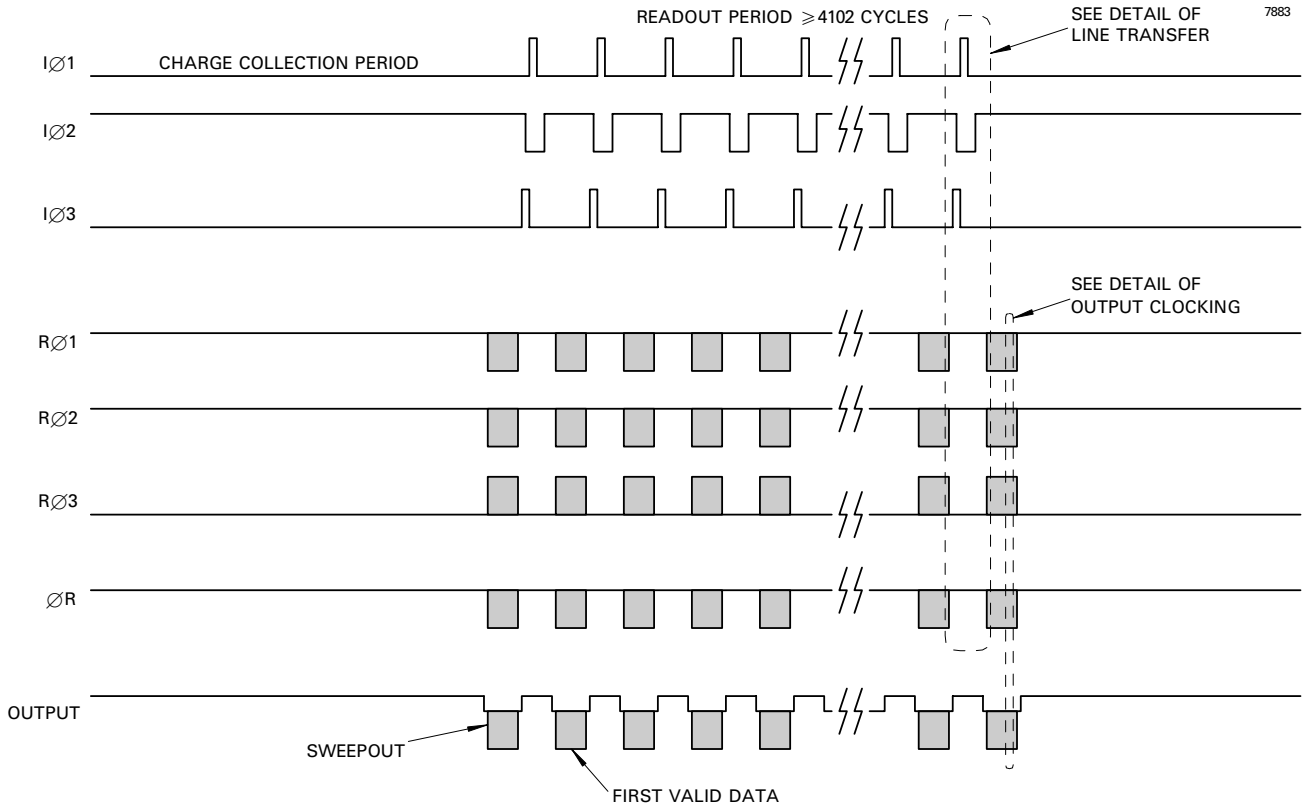
Detail of FET Buffer



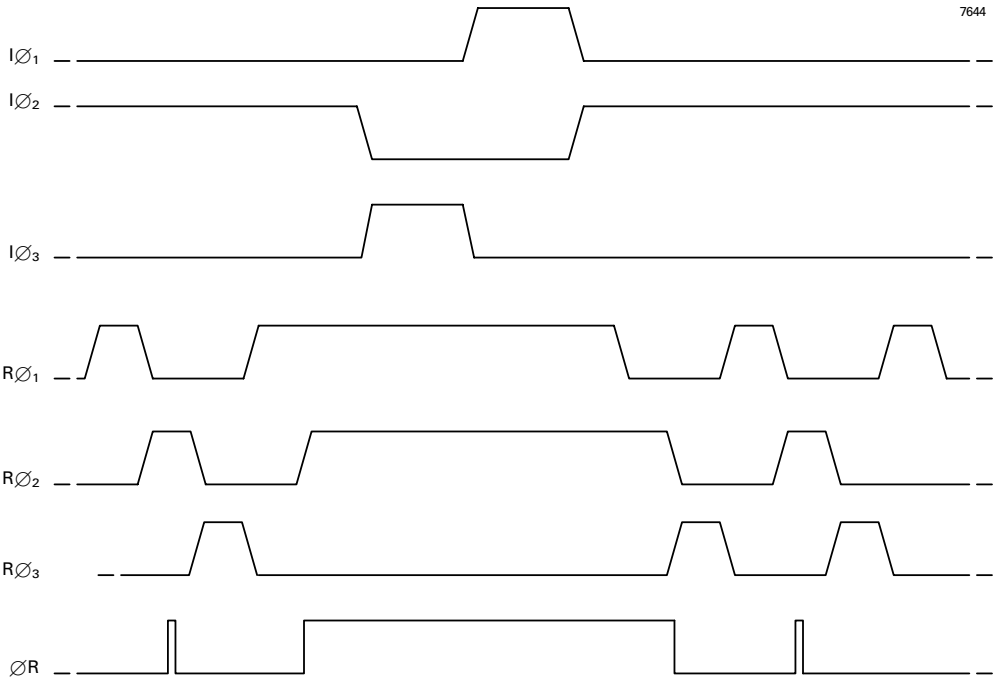
OUTPUT CIRCUIT



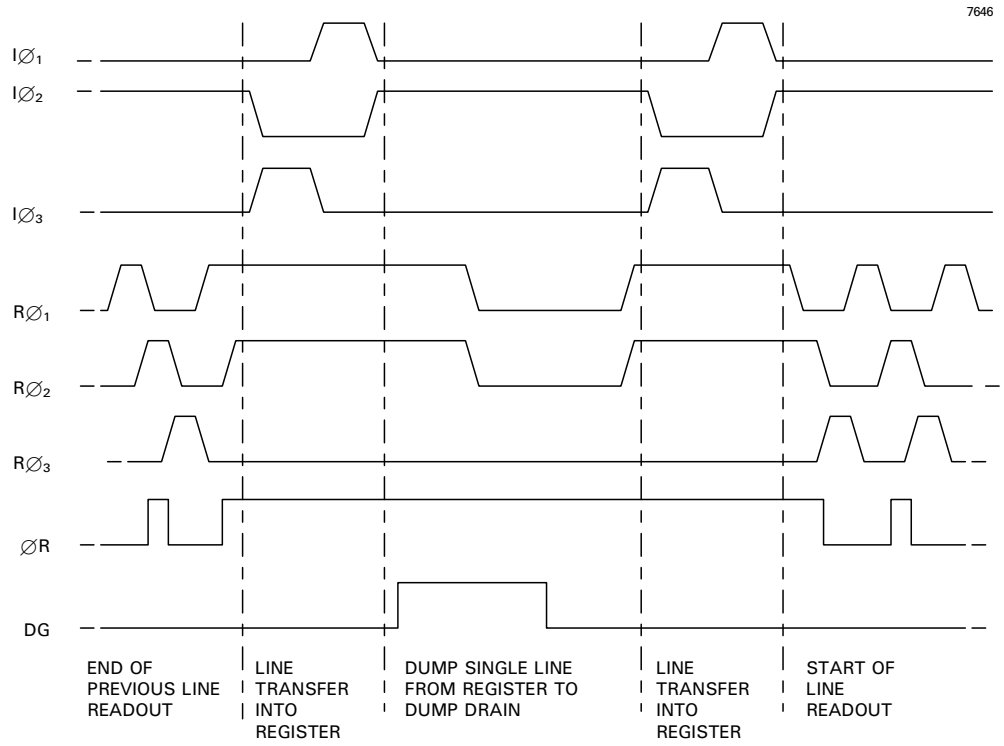
FRAME READOUT TIMING DIAGRAM



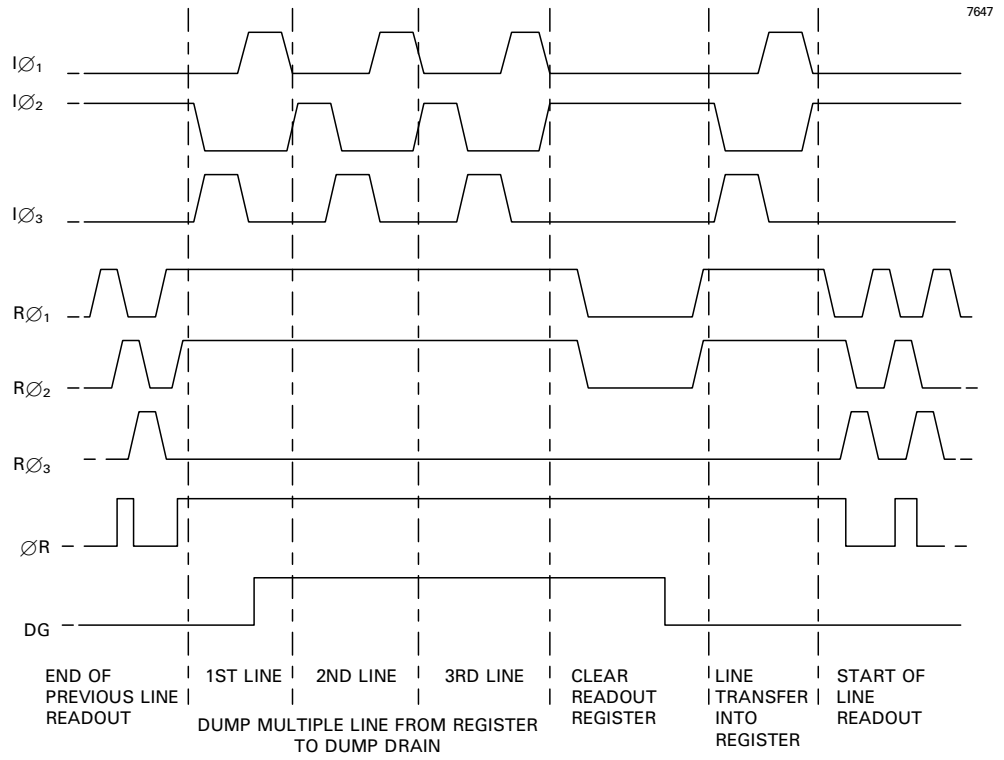
DETAIL OF LINE TRANSFER



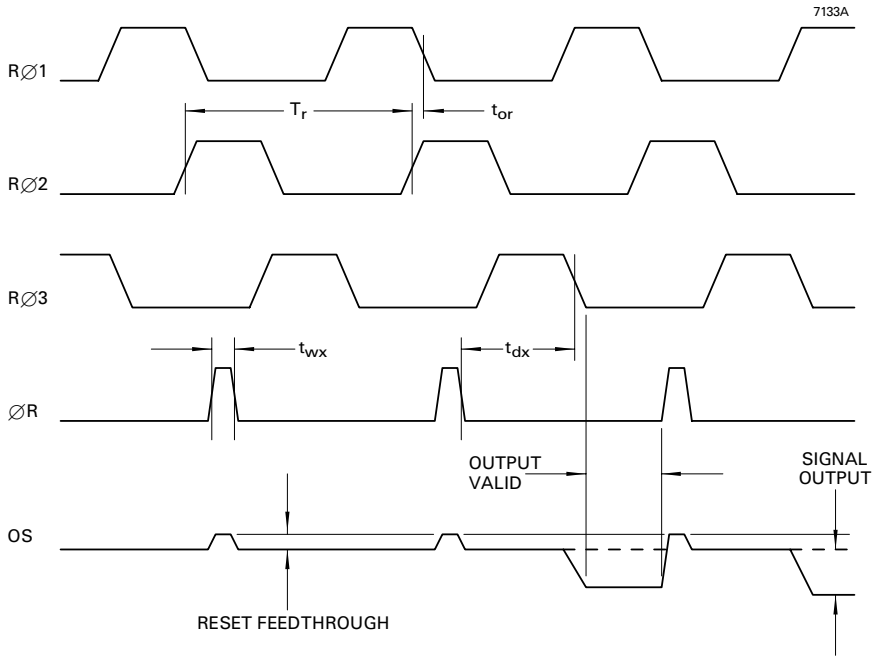
DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



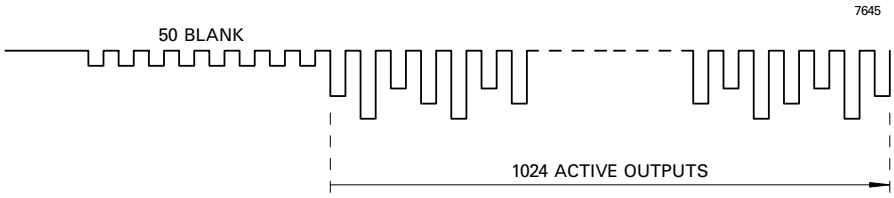
DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



DETAIL OF OUTPUT CLOCKING (Operation through both outputs)



LINE OUTPUT FORMAT (Split read-out operation)



CLOCK TIMING REQUIREMENTS

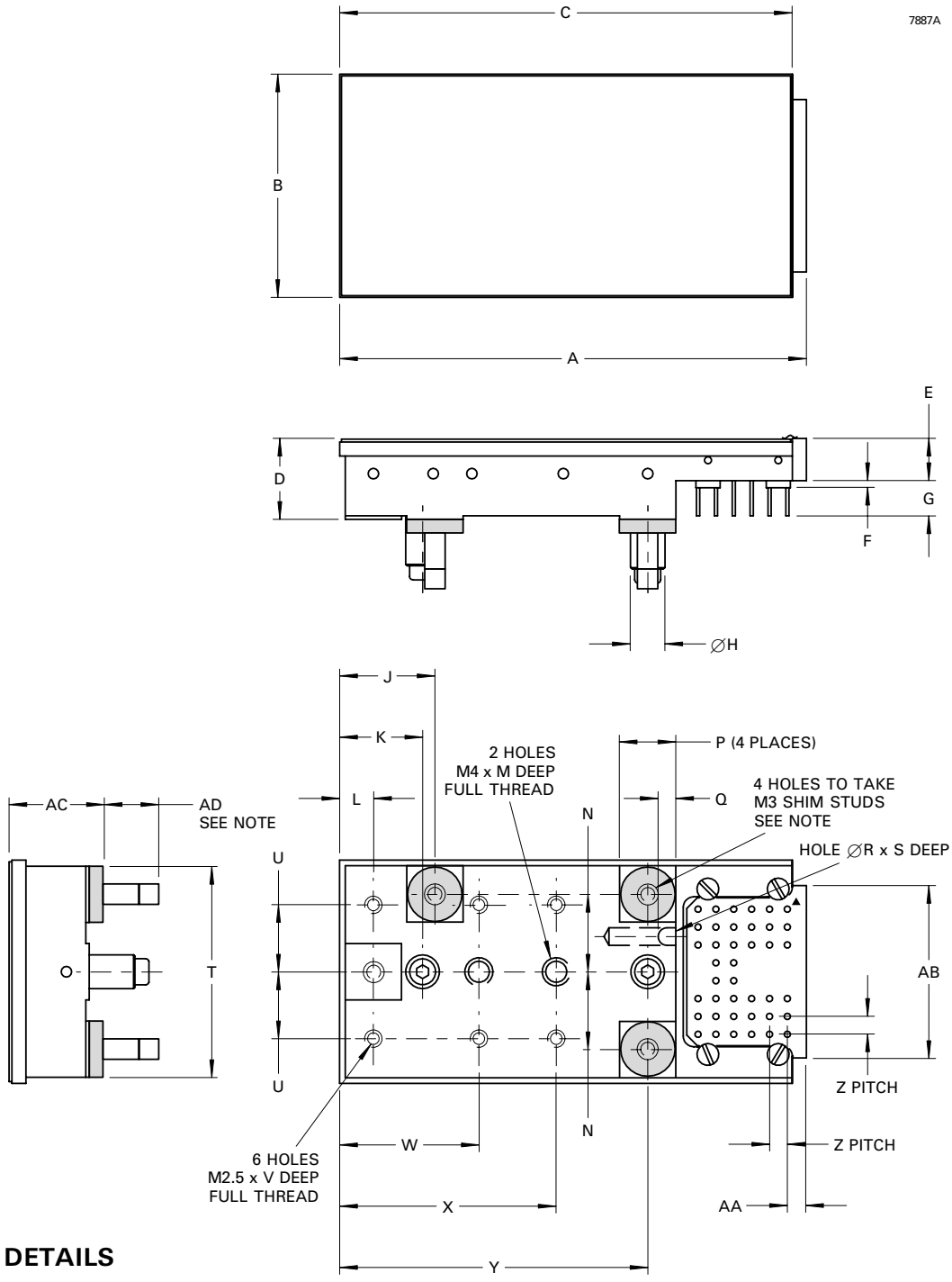
Symbol	Description	Min	Typical	Max	
T_i	Image clock period	50	100	see note 12	µs
t_{wi}	Image clock pulse width	25	50	see note 12	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	10	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	10	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	5	10	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	10	20	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	10	20	see note 12	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	see note 12	µs
T_r	Output register clock cycle period	1	see note 13	see note 12	µs
t_{rr}	Clock pulse rise time (10 to 90%)	100	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	50	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	50	$0.1T_r$	$0.2T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	50	$0.5T_r$	$0.8T_r$	ns

NOTES

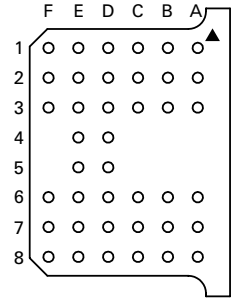
12. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
13. As set by the readout period.

OUTLINE
(All dimensions without limits are nominal)

Ref	Millimetres
A	66.64 max
B	31.72 ± 0.01
C	64.28 ± 0.01
D	11.65
E	6.00
F	1.00
G	5.00
H	4.800 ± 0.005
J	13.55
K	11.80
L	4.80
M	6.00 min
N	11.00
P	8.00
Q	2.50
R	2.50
S	6.50
T	30.00
U	9.50
V	5.50 min
W	19.80
X	30.80
Y	43.80
Z	2.54
AA	2.70
AB	24.5
AC	14.00 ± 0.01
AD	8.50 ± 0.01 15.00 ± 0.01



PIN CONNECTION DETAILS
(See page 5)



Outline Note

The device is supplied with shim studs to hold it onto the customer's mounting plate, fitted to three of the four holes as required. The studs are available in two lengths (see dimension AD). The default unless specified is the 8.50 mm stud in the offset position.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. The sensor is shipped with a shorting pad on the PGA for electrostatic protection. This must be removed before use. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (all CCD pins except V_{SS}, DD, RD, OD and OS) but not to the other pins. See also e2v technologies technical note TN906/419 for information about mosaic assembly.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 10^4 rads.

Certain characterisation data are held at e2v technologies. Users planning to use CCDs in a high radiation environment are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	–	373	K
Operating	153	173	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . . 5 K/min

MATING CONNECTOR

A custom ZIF connector is available for use with this sensor. The ZIF socket fits within the footprint of the package to optimise close-packing of mosaic assemblies. Contact e2v technologies for details.