e2v technologies

CCD57-10 AIMO Backthinned Compact Pack
High Performance CCD Sensor

FEATURES

- 512 by 512 Usable Pixels
- Image Area 6.7 x 6.7 mm
- Back Illuminated Format
- Frame Transfer Operation
- 13 μm Square Pixels
- Symmetrical Anti-static Gate Protection
- Very Low Noise Output Amplifiers
- Gated Dump Drain on Output Register
- 100% Active Area
- Advanced Inverted Mode Operation (AIMO)
- New Compact Footprint Package

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- Star Tracking
- Medical Imaging

INTRODUCTION

This version of the CCD57 family of sensors has frame transfer architecture. Back illumination technology, in combination with extremely low noise amplifiers, makes the device well suited to the most demanding scientific applications. To improve the sensitivity further, the CCD is manufactured without anti-blooming structures.

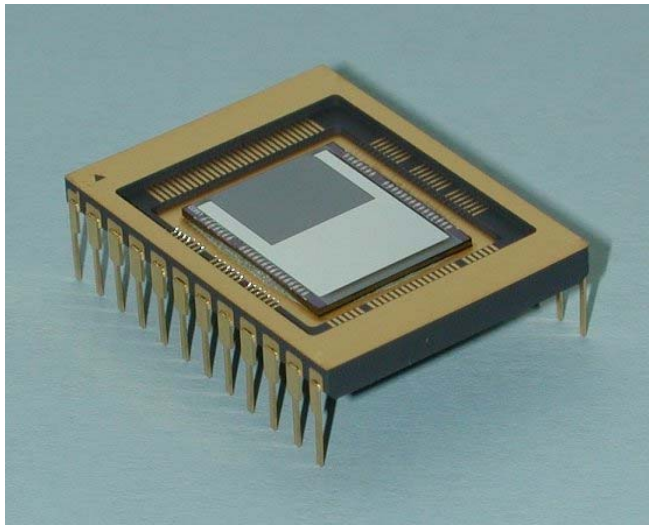
This device has a single serial output register. Separate charge detection circuits are incorporated at each end of the register, which is split so that a line of charge can be transferred to either output, or split between the two.

The register is provided with a drain and control gate along the outer edge of the channel for charge dump purposes.

The sensor is made using e2v technologies' Advanced Inverted Mode process to minimise dark current, allowing the device to be operated with extended integration periods and minimal cooling.

Other variants of the CCD57-10 available are front illuminated format and non-inverted mode. In common with all e2v technologies CCD Sensors, the CCD57-10 is also available with a fibre-optic window or taper, or with a phosphor coating.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

Maximum readout frequency	3	MHz
Output responsivity	6	$\mu V/e^-$
Peak signal	100	ke^-/pixel
Dynamic range (at 20 kHz)	~33 333:1	
Spectral range	200 - 1100	nm
Readout noise (at 20 kHz)	2.0	e^- rms

GENERAL DATA

Format

Image area	6.656 x 6.656	mm
Total elements (H)	536	
(V)	528	
Active pixels (H)	512	
(V)	512	
Storage area:		
Total elements (H)	536	
(V)	528	
Pixel size	13 x 13	μm

Additional pixels are provided in the image area and output register for over-scanning purposes.

Number of output amplifiers	2	
Weight (approx, no window)	6	g

Package

Package size	22.6 x 29.9	mm
Number of pins	24	
Inter-pin spacing	2.54	mm
Window material	quartz or removable glass	
Type	ceramic DIL array	

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PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	60k	100k	-	e^-/pixel
Peak output voltage (no binning)	-	600	-	mV
Dark signal at 293 K (see notes 2 and 3)	-	250	500	e^-/pixel/s
Dynamic range (see note 4)	-	33333:1	-	
Charge transfer efficiency (see note 5): parallel serial	 - -	 99.9999 99.9993	 - -	 % %
Output amplifier responsivity (see note 3)	4.0	6.0	8.0	$\mu V/e^-$
Readout noise at 253 K (see notes 3 and 6)	-	3.0	4.0	rms e^-/pixel
Maximum readout frequency (see note 7)	-	3.0	-	MHz
Dark signal non-uniformity at 293 K (std. deviation) (see notes 3 and 8)	-	60	125	e^-/pixel/s

Spectral Response (at 253 K)

Wavelength (nm)	Minimum Response (QE)						Response Non-uniformity (1σ)	
	Enhanced Process			Basic Process				
	Broadband Coated	Midband Coated	UV Coated	Broadband Coated	Midband Coated	Uncoated		
300	-	-	45	-	-	-	-	%
350	50	25	45	25	15	10	5	%
400	80	50	55	55	40	25	3	%
500	80	85	60	75	85	55	3	%
650	75	85	60	75	85	50	3	%
900	30	30	30	30	30	30	5	%

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level)

	Min	Typical	Max	
I∅/I∅ interphase and S∅/S∅ interphase	-	1.1	-	nF
I∅/SS and S∅/SS per phase: phases 1 and 3 phase 2	 - -	 1.3 2.2	 - -	 nF nF
R∅/R∅ interphase	-	30	-	pF
R∅/(SS + DG + OD) per phase	-	40	-	pF
∅R/SS	-	10	-	pF
Output impedance (at typ. operating condition)	-	300	-	Ω

NOTES

1. Signal level at which resolution begins to degrade.
2. Measured between 253 and 293 K and V_{SS} +9.5 V. Dark signal at any temperature T (kelvin) may be estimated from:

   $$Q_d/Q_{d0} = 1.14 \times 10^6 T^3 e^{-9080/T}$$

   where Q_{d0} is the dark signal at T = 293 K (20 °C).

   Note that this is the typical performance and some variation may be seen between devices. Below 230 K, additional dark current components with a weaker temperature dependence may become significant.
3. Test carried out at e2v technologies on all sensors.
4. Dynamic range is the ratio of full-well capacity to readout noise measured at 253 K and 20 kHz readout speed.
5. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
6. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 20 μs integration period.
7. Readout at speeds in excess of 3 MHz into a 15 pF load can be achieved but performance to the parameters given cannot be guaranteed.
8. Measured between 253 and 293 K, excluding white defects.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 253 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well.

White spots Are counted when they have a generation rate 125 times the specified maximum dark signal generation rate (measured between 253 and 293 K). The typical temperature dependence of white spot defects is different from that of the average dark signal and is given by:

$$Q_d / Q_{d0} = 122T^3 e^{-6400/T}$$

White column A column which contains at least 9 white defects.

Black column A column which contains at least 9 black defects.

GRADE	0	1	2
Column defects:			
black or slipped	0	3	10
white	0	0	1
Black spots	30	50	200
Traps > 200 e^-	1	2	5
White spots	20	30	50

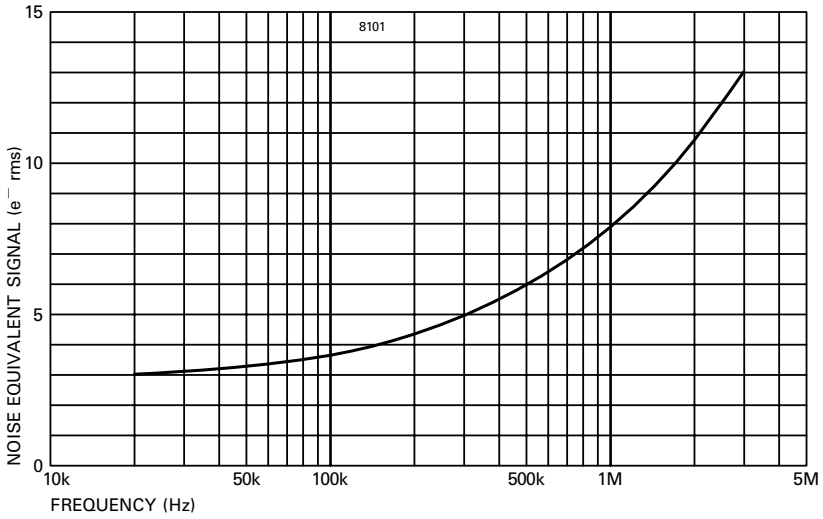
Grade 5 Devices which are fully functioning, with image quality below that of grade 2, and which may not meet all other performance parameters.

Minimum separation between
adjacent black columns . . . . . 50 pixels

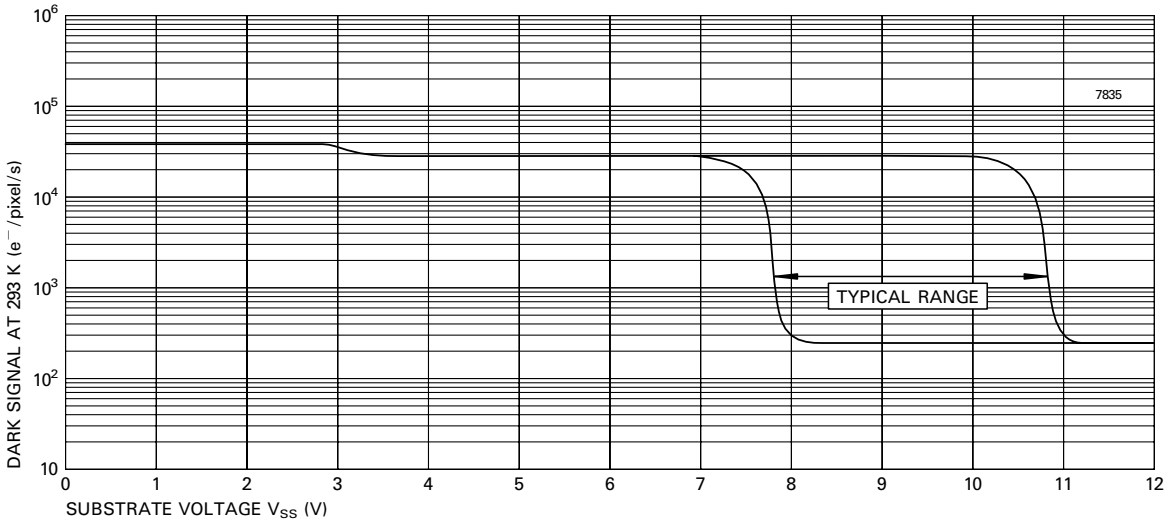
Note The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 253 K. The amplitude of white spots and columns will decrease rapidly with temperature.

TYPICAL OUTPUT CIRCUIT NOISE (Measured using clamp and sample)

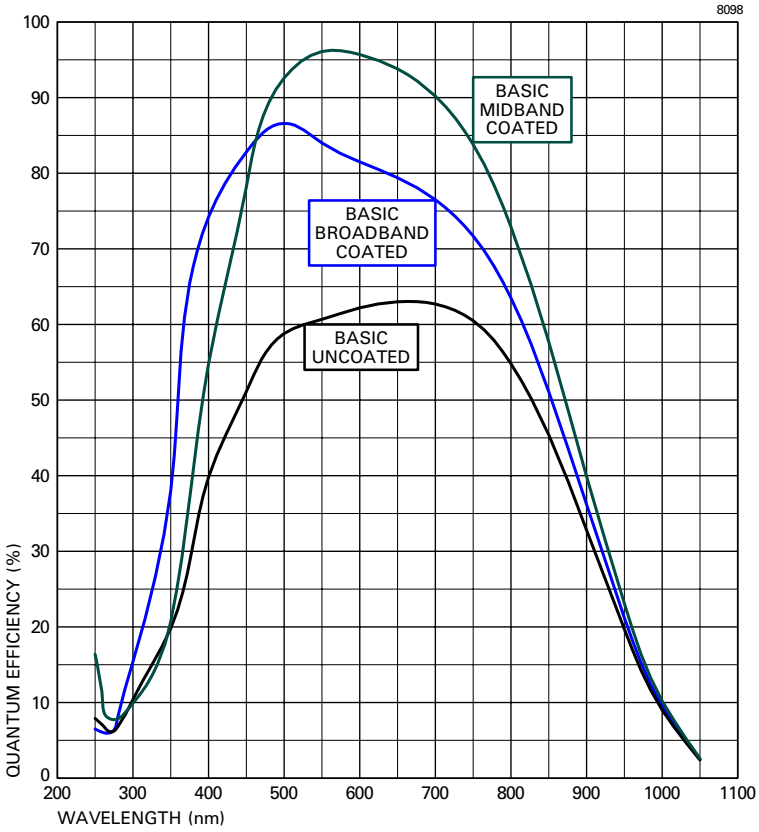
V_{SS} = 9.5 V V_{RD} = 17 V V_{OD} = 29 V

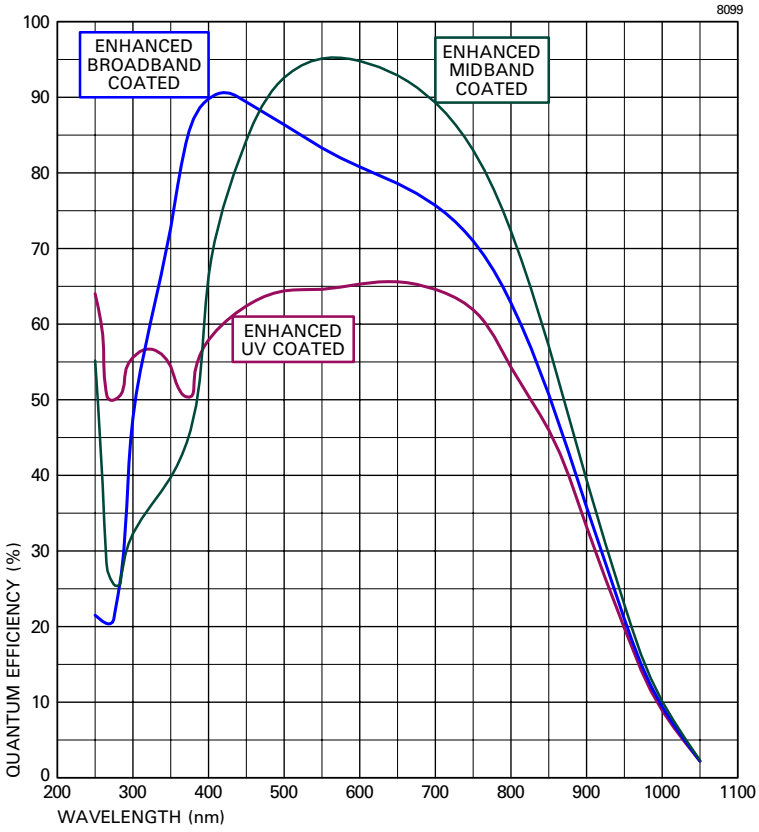


TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE

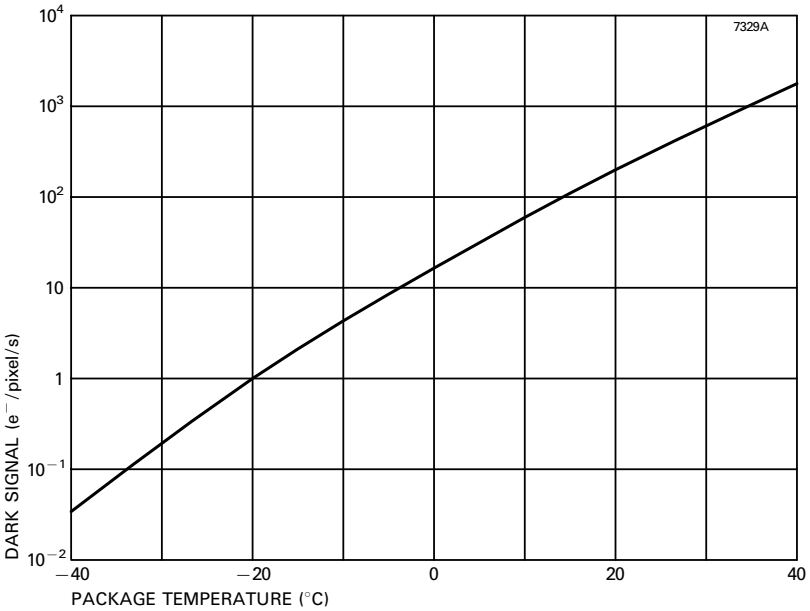


TYPICAL SPECTRAL RESPONSE (At −20 °C, no window)

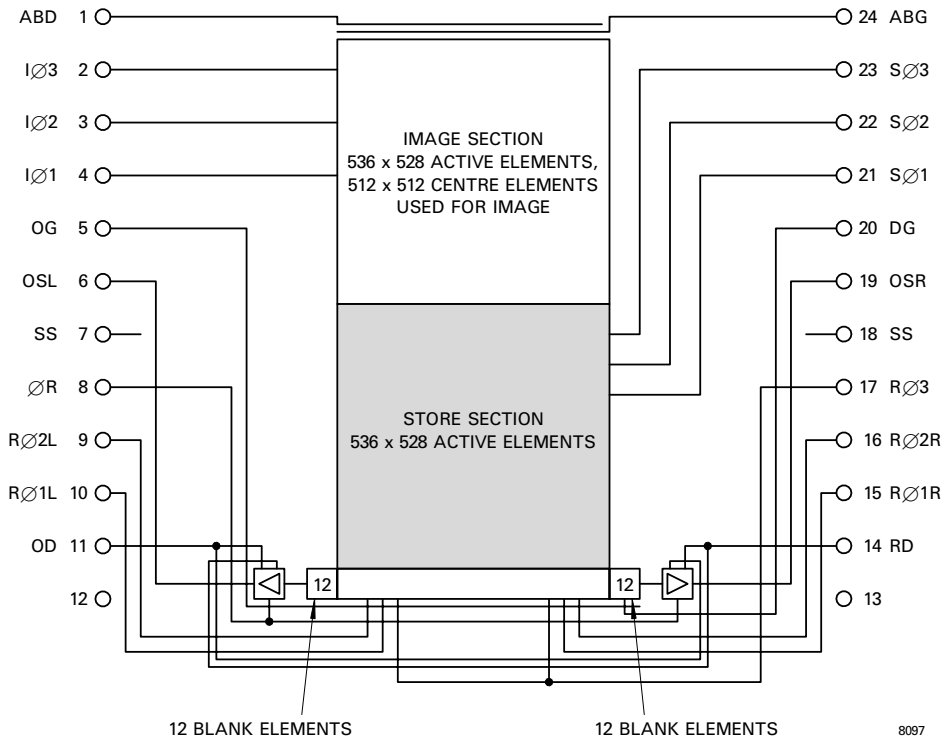




TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE (V_{SS} = +9.5 V)



DEVICE SCHEMATIC



Note Pins 12 and 13 are not connected. For convenience, the CCD57-10 Compact Pack is pin compatible with the CCD47-10 sensors in the compact pack, except that OSL = pin 12, OSR = pin 13 and pins 6 and 19 are not connected in the CCD47-10.

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

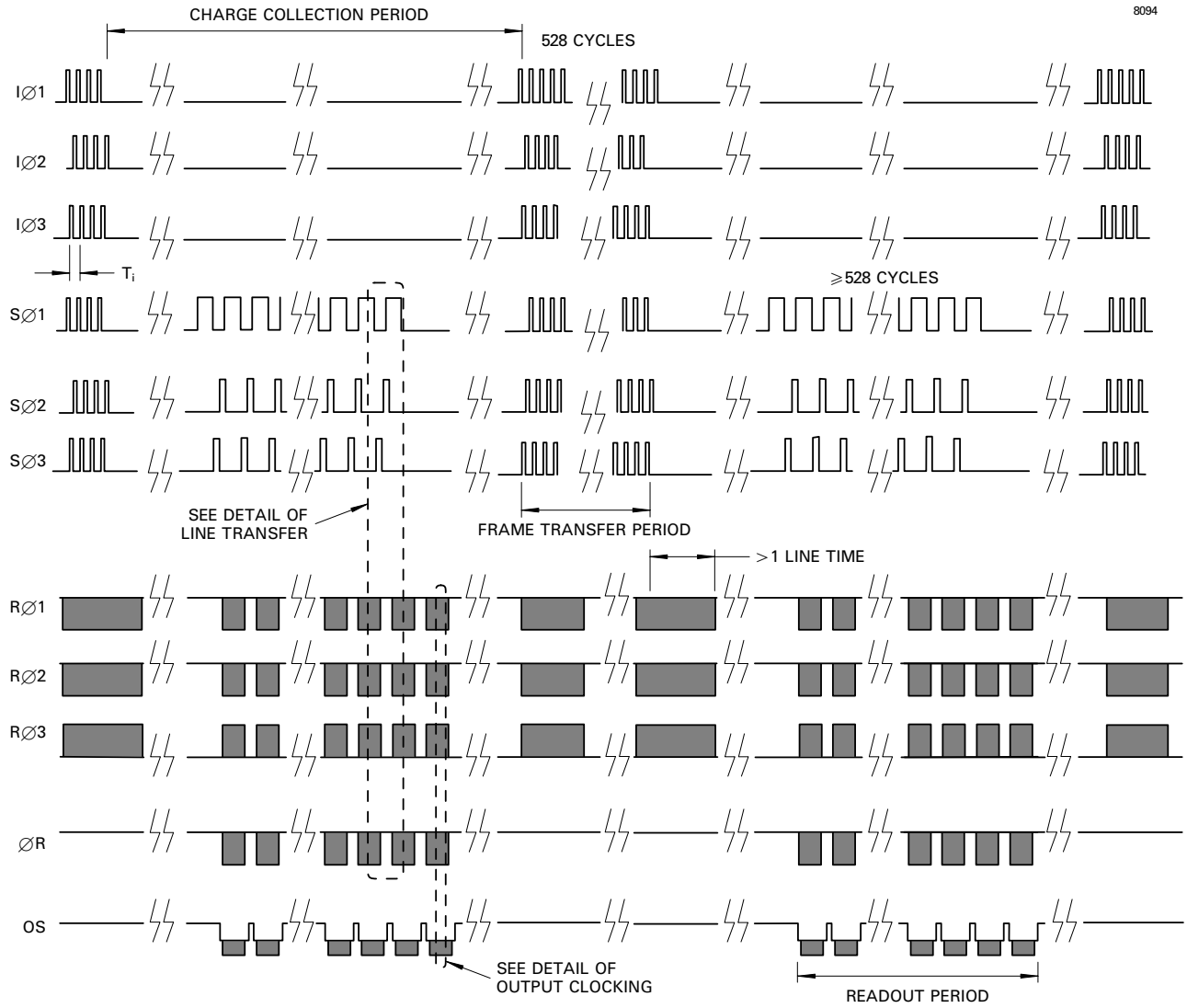
PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (See note 9) Min	Typical	Max	MAXIMUM RATINGS with respect to V_{SS}
1	ABD	Anti-blooming drain (see note 10)	17	24	V_{OD}	−0.3 to +25 V
2	I∅3	Image area clock	10	12	15	±20 V
3	I∅2	Image area clock	10	12	15	±20 V
4	I∅1	Image area clock	10	12	15	±20 V
5	OG	Output gate	1	3	5	±20 V
6	OSL	Output transistor source (left amplifier)	see note 11			−0.3 to +25 V
7	SS	Substrate	8	9.5	11	-
8	∅R	Output reset pulse (left and right amplifiers)	8	12	15	±20 V
9	R∅2L	Output register clock (left section)	8	10	15	±20 V
10	R∅1L	Output register clock (left section)	8	10	15	±20 V
11	OD	Output transistor drain (left and right amplifiers)	27	29	32	−0.3 to +35 V
12	-	No connection	-			-
13	-	No connection	-			-
14	RD	Reset transistor drain (left and right amplifiers)	15	18	21	−0.3 to +25 V
15	R∅1R	Output register clock (right section)	8	10	15	±20 V
16	R∅2R	Output register clock (right section)	8	10	15	±20 V
17	R∅3	Output register clock (left and right sections)	8	10	15	±20 V
18	SS	Substrate	8	9.5	11	-
19	OSR	Output transistor source (right amplifier)	see note 11			−0.3 to +25 V
20	DG	Dump gate (see note 12)	-	0	-	±20 V
21	S∅1	Storage area clock	10	12	15	±20 V
22	S∅2	Storage area clock	10	12	15	±20 V
23	S∅3	Storage area clock	10	12	15	±20 V
24	ABG	Anti-blooming gate	0	0	5	±20 V

Maximum voltages between pairs of pins:
pin 10 (OSL) to pin 11 (ODL) . . . . . ±15 V
pin 22 (ODR) to pin 23 (OSR) . . . . . ±15 V
Maximum output transistor current . . . . . 10 mA

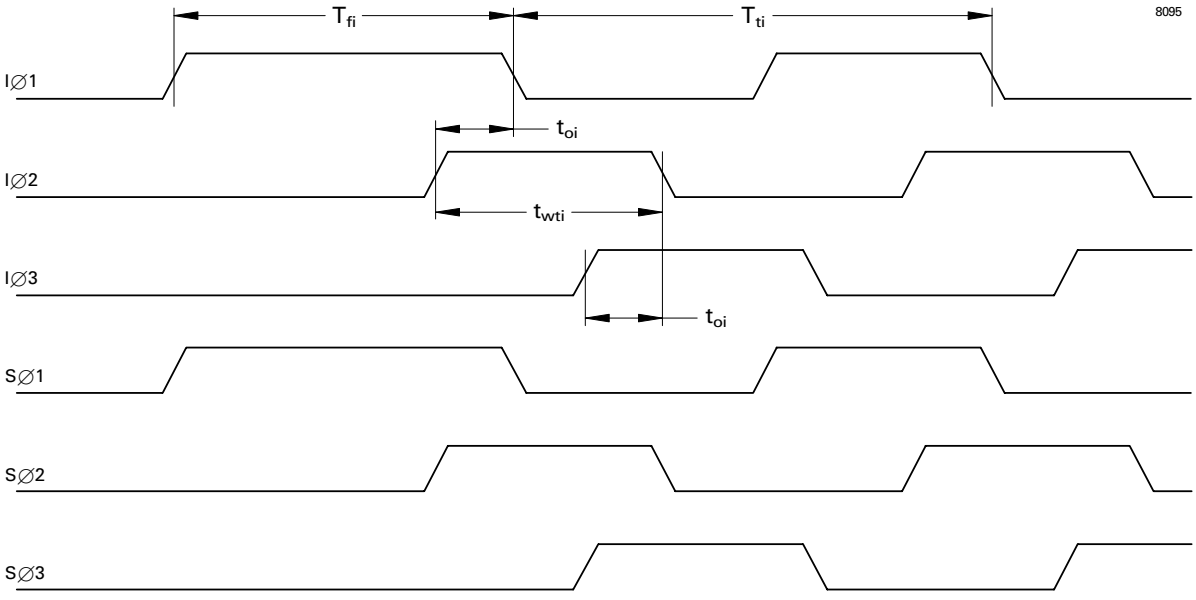
NOTES

9. Readout register clock pulse low levels +1 V; other clock low levels 0 ± 0.5 V.
10. Drain not incorporated, but bias is still necessary.
11. 3 to 5 V below OD. Connect to ground using a 3 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).
12. Non-charge dumping level shown. For operation in charge dumping mode, DG should be pulsed to 12 ± 2 V.
13. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.
14. With the R∅ connections shown, the device will operate through the right-hand output only. In order to operate from both outputs R∅1(L) and R∅2(L) should be reversed. Thus for right-hand output, connect pin 9 = pin 16 = R∅2, pin 10 = pin 15 = R∅1, pin 17 = R∅3 (common). For left-hand output, connect pin 9 = pin 16 = R∅1, pin 10 = pin 15 = R∅2. For split output, connect pin 9 = pin 15 = R∅1, pin 10 = pin 16 = R∅2. Use clock sequence R∅1:R∅2:R∅3, as shown in the following timing diagrams.

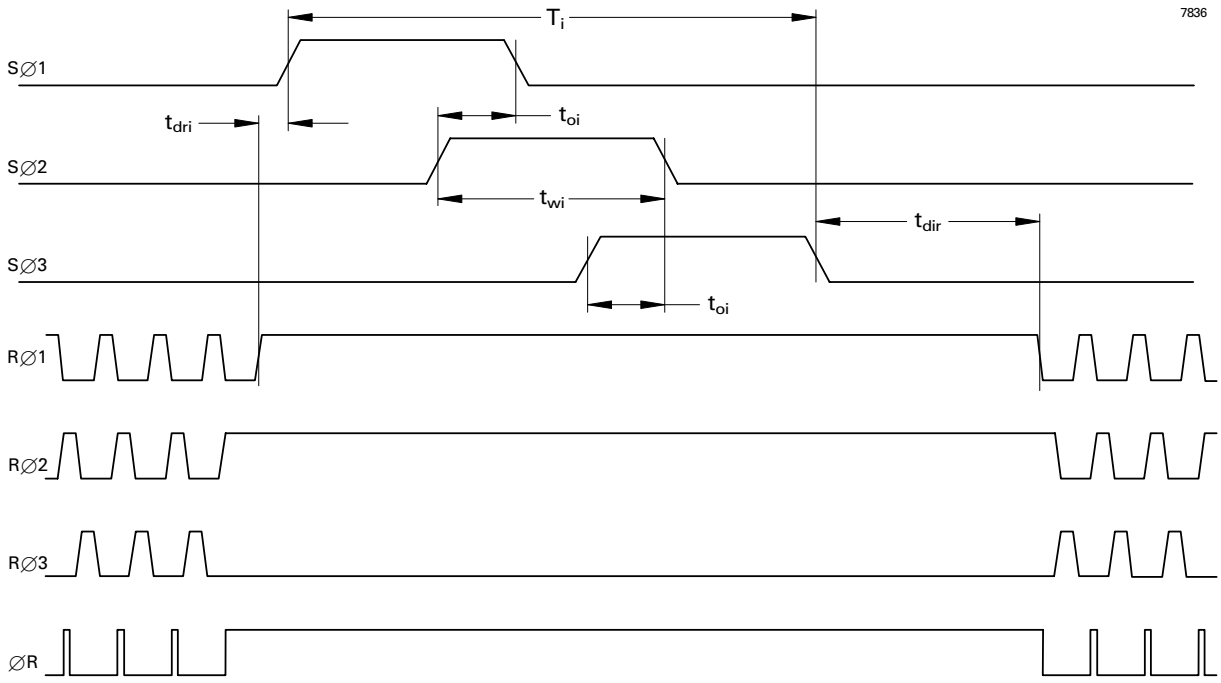
FRAME TRANSFER TIMING DIAGRAM



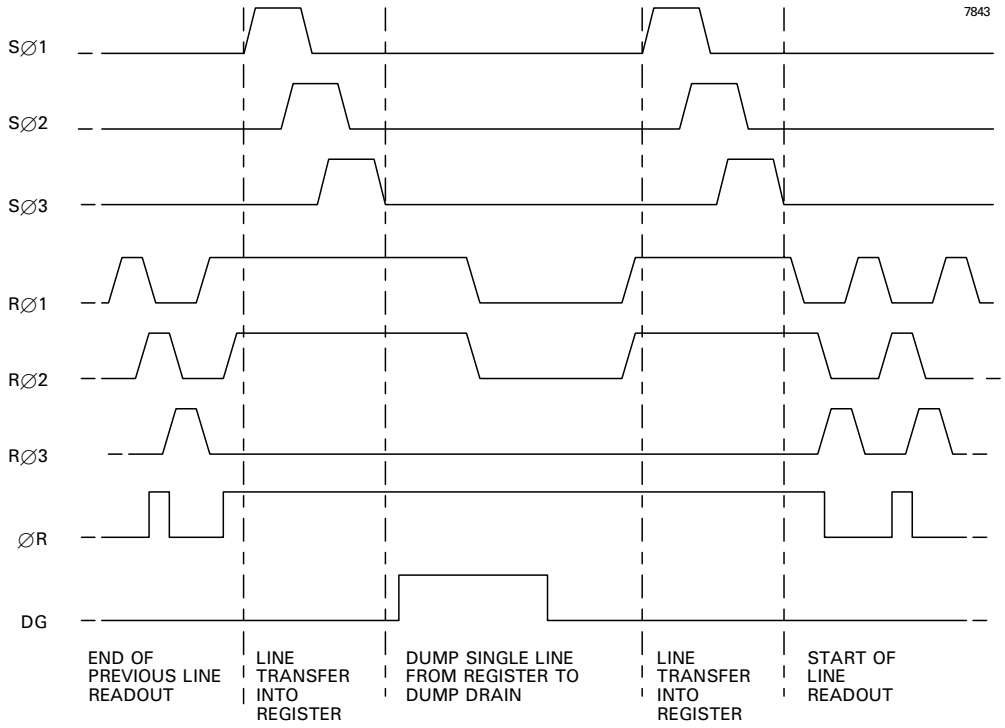
DETAIL OF FRAME TRANSFER



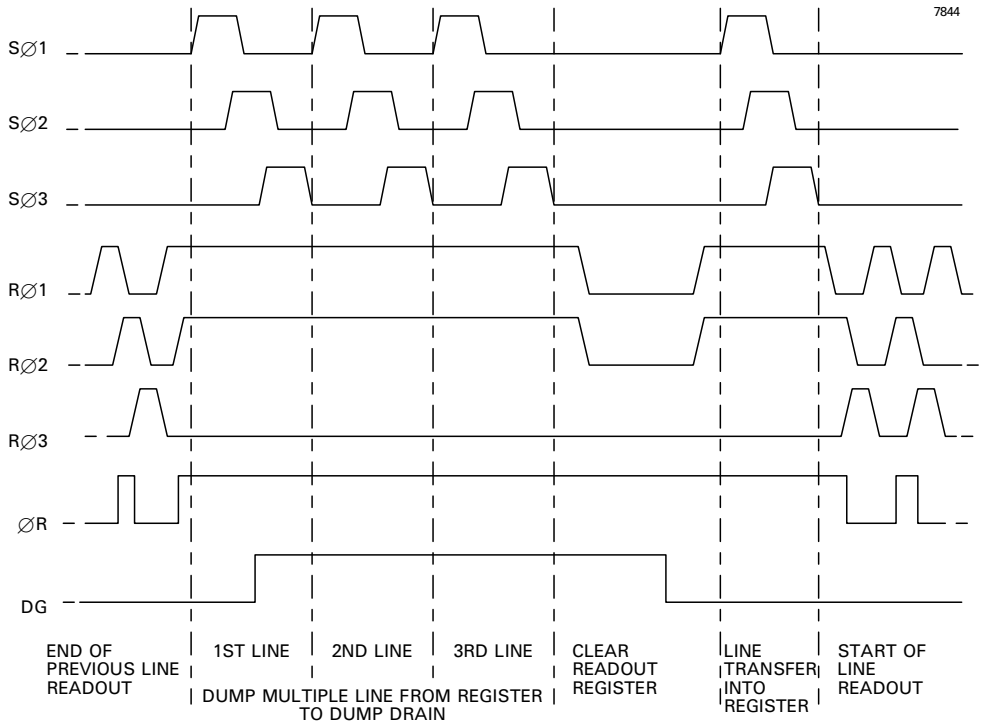
DETAIL OF LINE TRANSFER
(For output from a single amplifier)



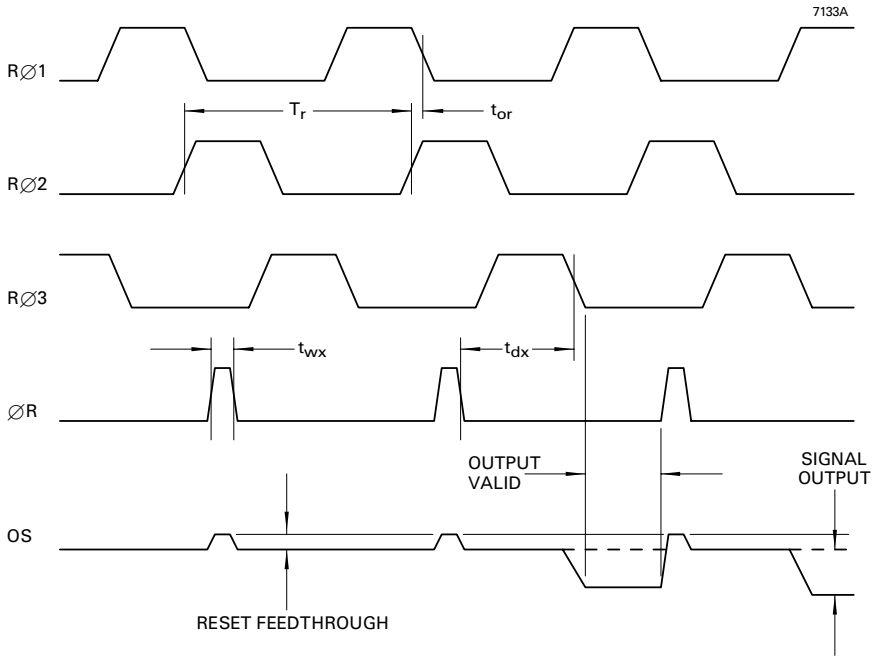
DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



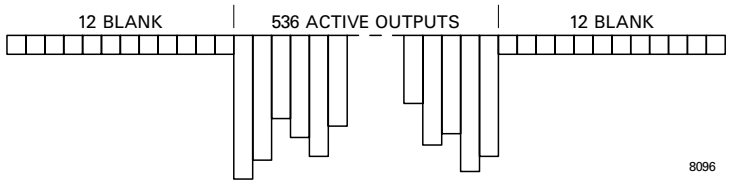
DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



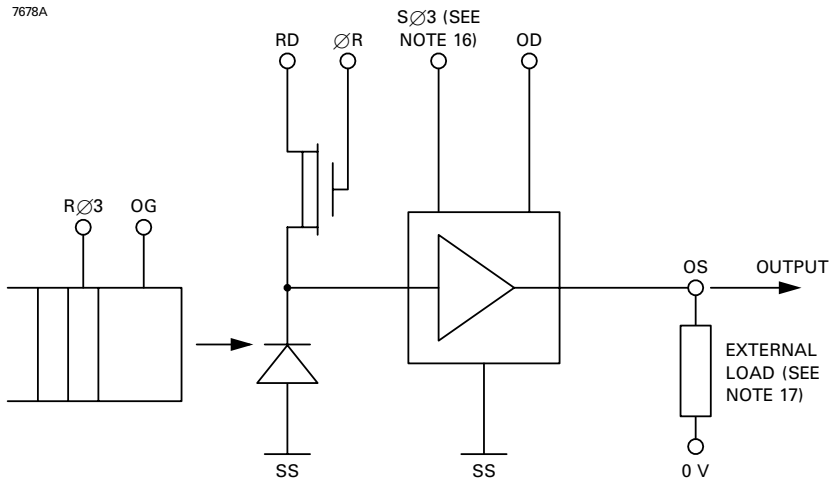
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_{fi}	First frame transfer pulse width	100	150	see note 15	µs
T_{ti}	Frame transfer clock period	2	5	see note 15	µs
t_{wti}	Frame transfer image clock pulse width	1	2	$T_{ti}/3 + t_{oi}$	µs
T_i	Store clock period	25	50	see note 15	µs
t_{wi}	Image/store clock pulse width	8	16	see note 15	µs
t_{ri}	Image/store clock pulse rise time (10 to 90%)	0.03	0.1	$0.2T_{ti}$	µs
t_{fi}	Image/store clock pulse fall time (10 to 90%)	t_{ri}	0.1	$0.2T_{ti}$	µs
t_{oi}	Image/store clock pulse overlap	0.2	0.3	$0.2T_{ti}$	µs
t_{dir}	Delay time, SØ stop to RØ start	1	2	see note 15	µs
t_{dri}	Delay time, RØ stop to SØ start	1	1	see note 15	µs
T_r	Output register clock cycle period	200	1000	see note 15	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

15. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

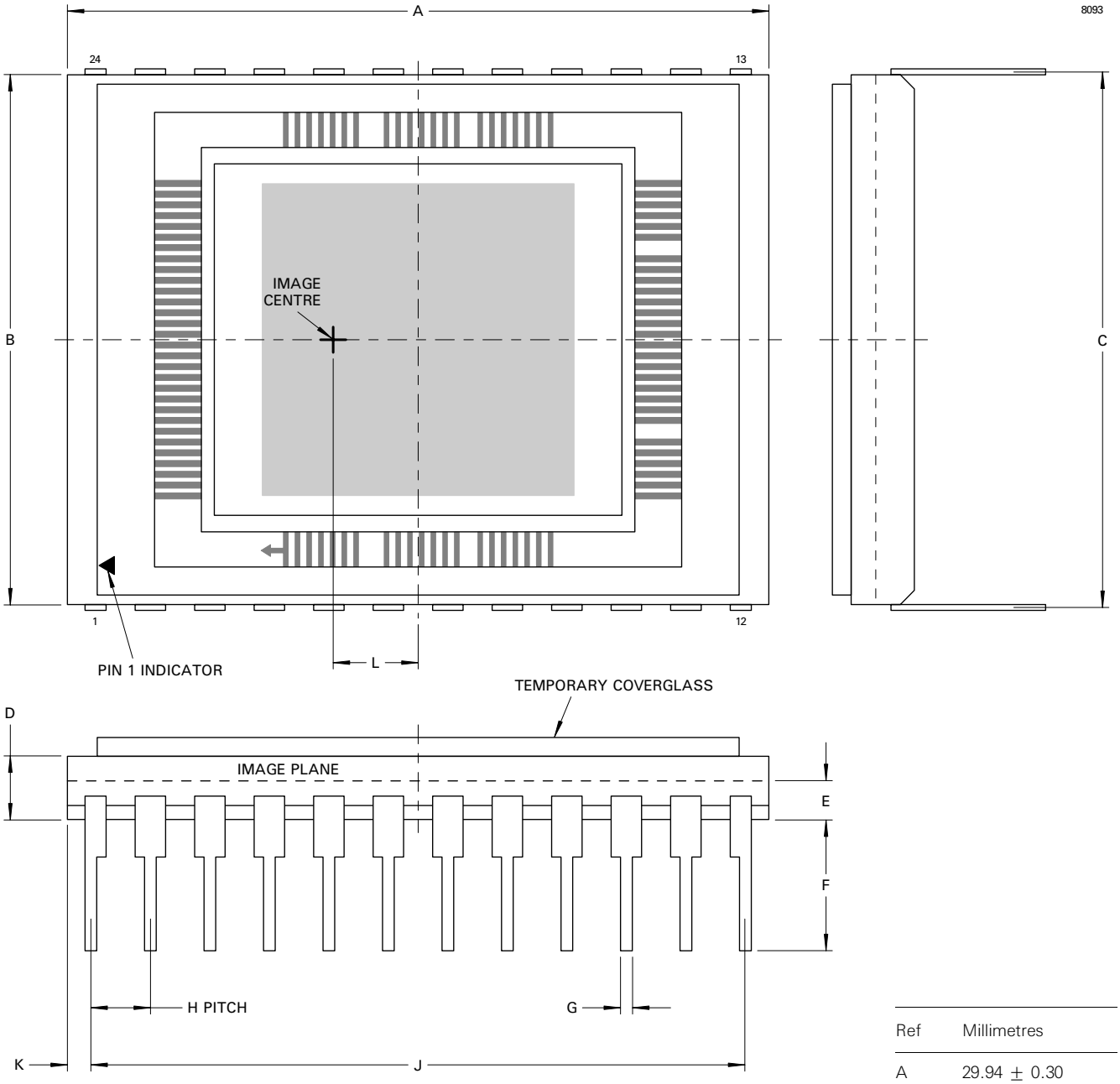
OUTPUT CIRCUIT



NOTES

16. The amplifier has a DC restoration circuit which is internally activated whenever S∅3 is high.
17. Not critical; can be a 3 to 5 mA constant current supply or an appropriate load resistor.

OUTLINE
(All dimensions without limits are nominal)



Ref	Millimetres
A	29.94 ± 0.30
B	22.61 ± 0.25
C	22.86 ± 0.25
D	2.70 ± 0.27
E	1.65 ± 0.25
F	5.6 ± 0.5
G	0.46 ± 0.05
H	2.54 ± 0.13
J	27.94 ± 0.13
K	1.0 ± 0.3
L	3.6 ± 0.3

ORDERING INFORMATION

Options include:

- Temporary Quartz Window
- Permanent Quartz Window
- Temporary Glass Window
- Permanent Glass Window
- Fibre-optic Coupling
- UV Coating
- X-ray Phosphor Coating

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 5, 8, 9, 10, 15, 16, 17, 20, 21, 22, 23, 24) but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 10^4 rads.

Certain characterisation data are held at e2v technologies. Users planning to use CCDs in a high radiation environment are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	–	373	K
Operating	153	273	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . . . 5 K/min