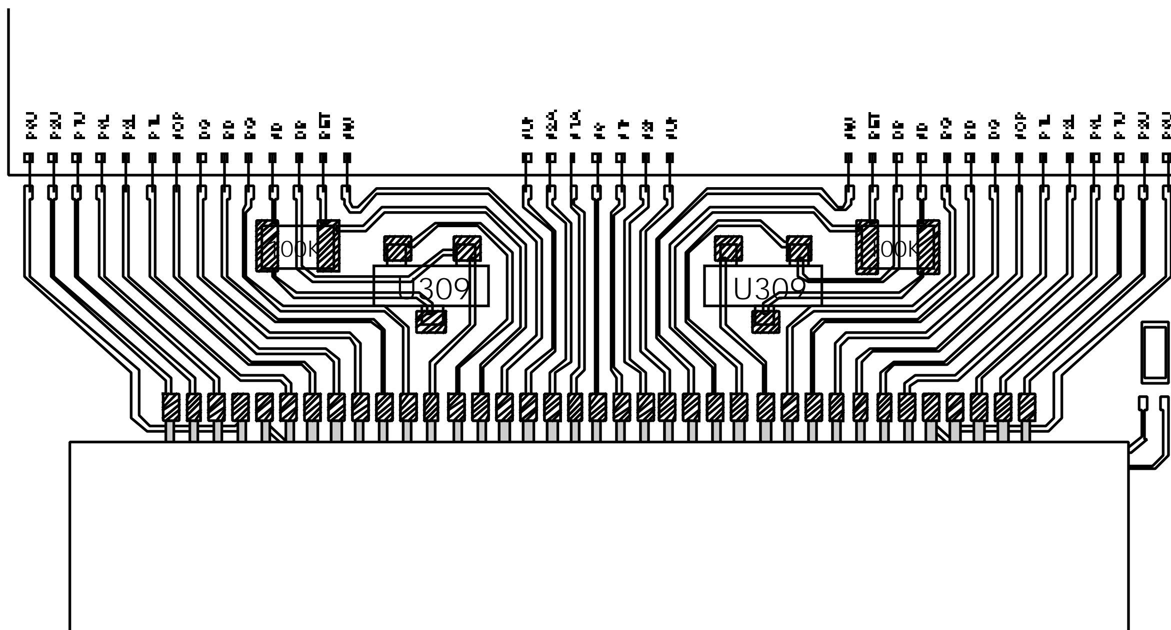
Figure 10. Plot of the metallization and components on the AlN, and the pads and bond wires on the CCD.



Device operation

The following are typical voltage settings for the device that we use in wafer probing, as well as minimum and maximum values beyond which the device has not been screened and therefore could be damaged. The gate voltages can be varied over a wide range, and one needs to experiment to find settings that yield acceptable CTI, high full well, low spurious charge and low dark current. The gate voltage at which the surface inverts is typically about -6 V and varies with wafer lot by a volt or so. The asterisk for the minimum and maximum gate voltages means that these gates are tested for shorts at wafer probe to voltages of +20 and -20 with respect to substrate and with respect to gates that they overlap. Thus, if P1 were at -10V, then P2 or P3 should not exceed +10 V.

Function	Typical value(s)	Minimum value	Maximum value
P1, P2, P3	-6, +4	-20*	20*
S1, S2, S3, SW	-2, +8	-20*	20*
OG	0	-20*	20*
RG	3, 10	-20	20
SCP	10	0	15
RD	10 – 12	0	20
DR	18 – 20	0	20
SUB	0 (system ground)		

Nanonics pin no.	Device function	Mnemonic
1	Parallel-2 upper	P2U
2	Parallel-1 upper	P1U
3	Parallel-3 lower	P3L
4	Parallel-3 upper	P3U
5	Temperature sensor	TS
6	Parallel-2 lower	P2L
7	Parallel-1 lower	P1L
8	Scupper	SCP
9	Output gate	OG
10	Reset drain	RD
11	Reset gate	RG
12	Drain	DR
13	Video output	OUT
14	Video return	RET
15	Summing well	SW
16	Substrate	SUB
17	Serial-2, A	S2A
18	Serial-1, A	S1A
19	Serial-3	S3
20	Serial-1, B	S1B
21	Serial-2, B	S2B
22	Substrate	SUB
23	Summing well	SW
24	Video return	RET
25	Drain	DR
26	Video output	OUT
27	Reset gate	RG
28	Reset drain	RD
29	Output gate	OG
30	Scupper	SCP
31	Parallel-1, lower	P1L
32	Parallel-2, lower	P2L
33	Temperature sensor	TS
34	Parallel-3, upper	P3U
35	Parallel-3 lower	P3L
36	Parallel-1, upper	P1U
37	Parallel-2, upper	P2U

Table 1. Pinouts for the Nanonics connector. The device functions appear on the same pins on the two connector.

A photograph of a packaged device together with the flexprint is shown in Figure 7. Currently all devices come with the flexprint and a mating Nanonics connector on one end and a mini-D connector on the other. The latter is a larger and more robust connector on the end to which the driving circuits are connected. This eliminates the risk of possible damage to the smaller connector on the package, since the user needs only deal with the larger connector on the flexprint. The table on the next page lists the pinouts for both the small connector on the package itself and for the larger connector attached to the flexprint.

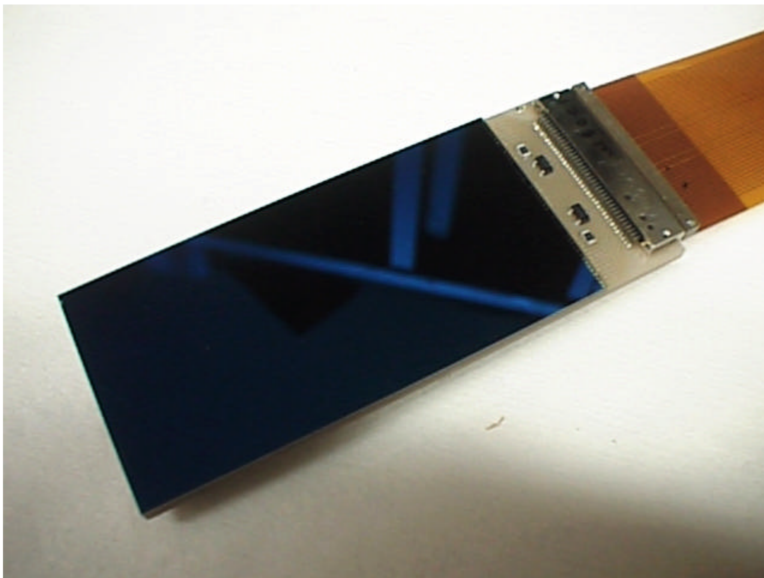


Figure 7. Photograph of a device mounted in a U. of Hawaii package.

Figure 10 below shows the layout of the metallization on the AlN substrate and the bonding diagram for the chip.

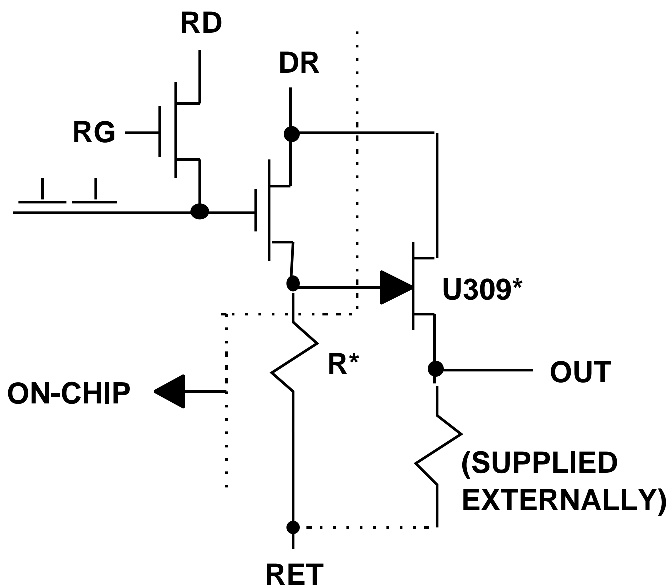


Figure 8. Schematic of the output circuit including the JFET buffer.

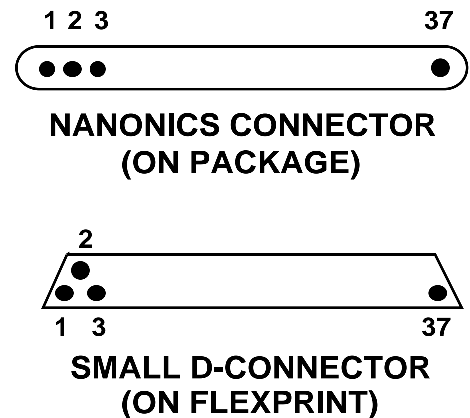


Figure 9. Pin number assignments for the Nanonics connector on the package and the D-connector on the flexprint.

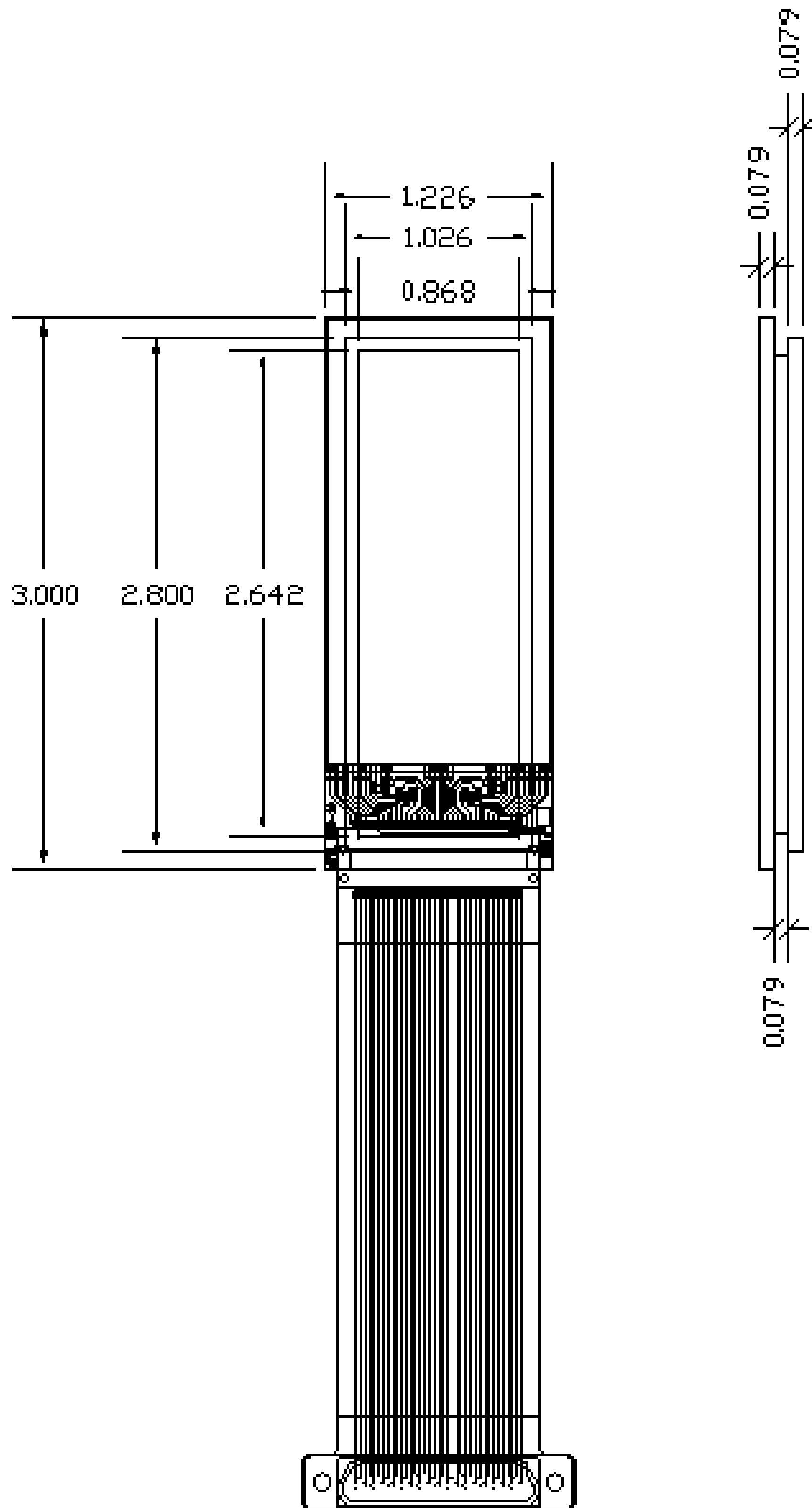


Figure 6. Engineering drawing of the device package

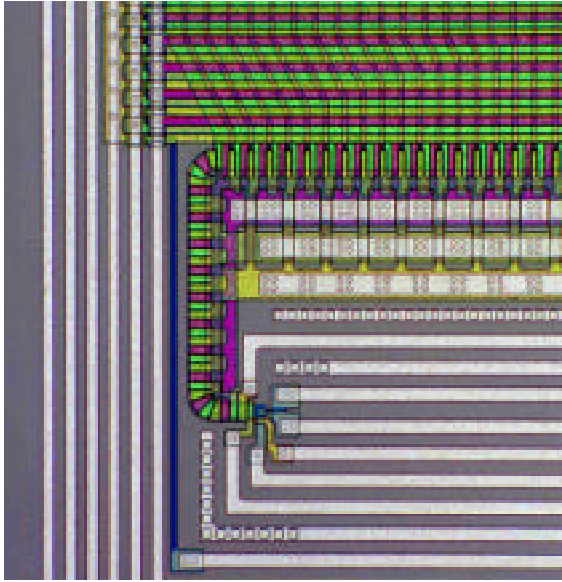


Figure 5. Photograph showing the region depicted in Figure 4.

in trying to funnel the charge into the narrow output node. Figure 5 shows a photograph of the region depicted by Figure 4.

The output circuit is a conventional floating diffusion amplifier, or gated charge integrator. The load resistor R for the sense MOSFET must be located off-chip, and a value of 100 k is currently used. The conversion sensitivity of this circuit is approximately 15-20 $\mu V/e^-$. The signal from the MOSFET source is buffered by a second-stage source follower using a low-noise n-channel JFET (U309) mounted on the package. This allows one to drive the capacitance of the video line running from the package to the next stage of signal processing at data rates up to about 1 MHz. The load resistor for the JFET must be supplied external to the packaged. Figure 8 depicts the details of this arrangement.

Packaging

The package developed for this device is a custom design by Gerry Luppino of the U. of Hawaii. Figure 6 shows an engineering drawing of the package, and a photograph of a packaged device is shown in Figure 7. This package was designed to make large multi-chip focal-plane arrays of closely abutted devices. The base of the package consists of three slabs of aluminum nitride sandwiched together with epoxy. The two lower AlN slabs are smaller in area, with the middle one smaller in width and length than the remaining two. This provides a lip which can be used to clamp the package to a heat sink. Aluminum nitride was chosen for its excellent thermal conductivity and good thermal expansion match to silicon. The uppermost AlN supports the CCD and is designed so that the three abuttable edges of the device will be spaced slightly back from the AlN edge for protection of the sawn device edges. This piece has gold metallization traces that lead from the chip to a subminiature 37-pin Nanonics female connector. This connector requires considerable care when engaging and disengaging mating connectors.

The load resistors for the MOSFETs and U309 JFETs are surface-mount components and are soldered or epoxied to the AlN board. A silicon-diode temperature sensor is usually also mounted on the AlN.

directional charge transfer depending on the clocking applied to the S1 and S2 lines. Thus, with S1A tied to S1B and S2A tied to S2B the serial register clocks the left half of the image to the left output and the right half to the right output (Figure 2 left). With the S1 and S2 connections exchanged all charge can be clocked to the left (as shown) or to the right. Note that there is no transfer gate separating the parallel and serial registers.

Figure 4 depicts the region in the corner around the output circuit and shows both slanted outer columns and a 180° loop in the serial register. These features are necessary so that the parallel clock lines need not be pushed to the left to avoid the output amplifier and thereby increase the side-to-side chip spacing. The tapered section involves four extra rows of pixels in the parallel section. This figure illustrates the geometry of this taper design, which has been used several times on large-area imagers from Lincoln Laboratory. Each of the 17 columns involved lies on 15-μm centers at the top and tapers down to 13 μm before reaching the bottom. In this way we are able to push the serial register loop 17×2 or 34 μm to the right and gain the necessary spacing.

The narrowing of the CCD channel for these columns reduces the well capacity, so in compensation the vertical pixel pitch for the four extra rows is increased from 15 to 18 μm. In addition, the serial register has been made amply wide so that its capacity should exceed that of the imaging pixels.

The serial loop contains 10 extra delay stages between the first column and the output sense amplifier. The last gate of the 10th stage is labeled SW (for Summing Well) and is brought out on a separate lead for those who wish to do binning. For non-binned clocking this gate would be clocked as phase 3 (S3). It should be mentioned that the summing well will not hold any more charge than a pixel full well. Elongating this well in the direction of charge transfer might create CTE problems, while widening it would also introduce a similar problem

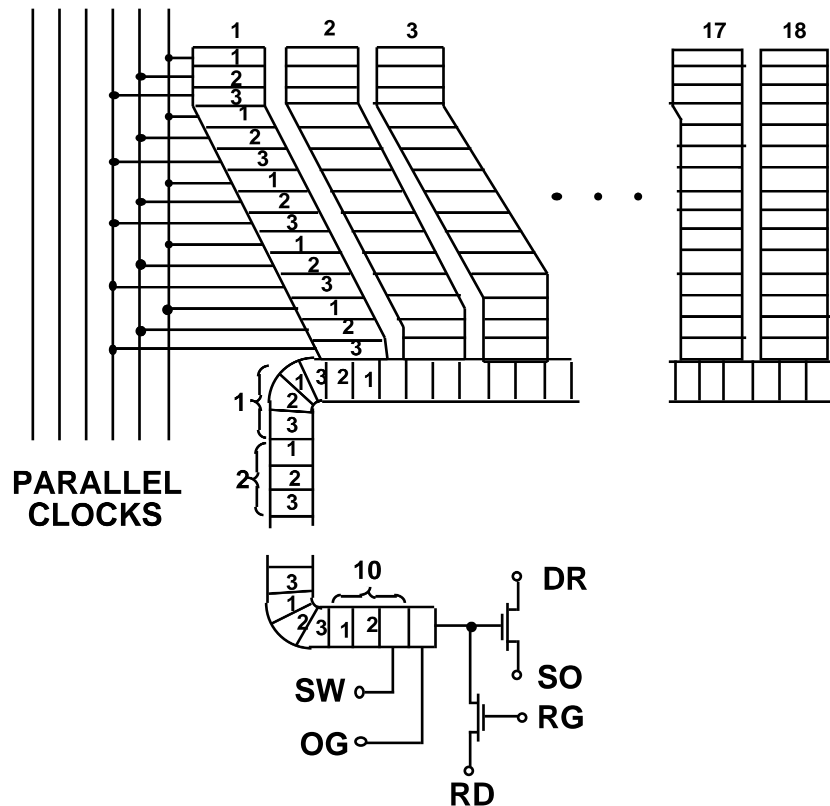


Figure 4. Depiction of the region around the output circuit.

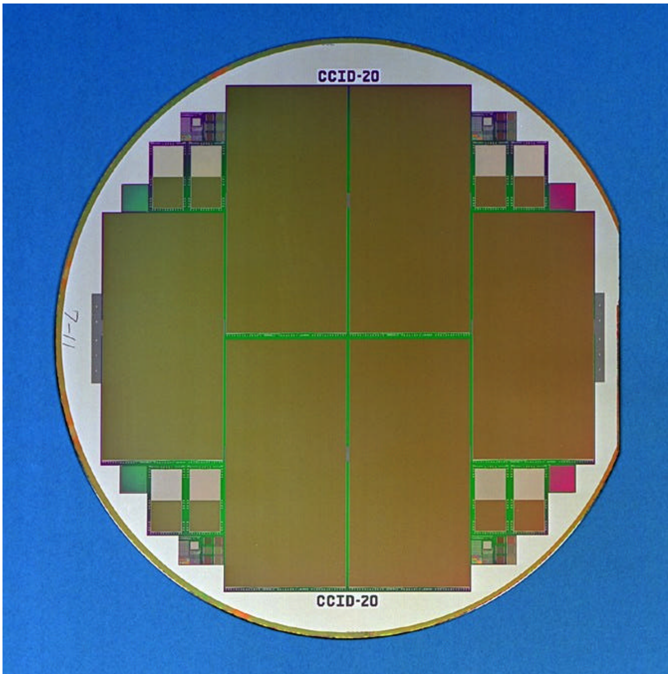


Figure 2. Photo of a 150-mm wafer with six 2k×4k imagers. Smaller devices around the periphery are test imagers and process control test structures.

The device is designed to have mirror symmetry about the center line, the principal motivation being that front- and back-illuminated versions of the device will look identical. Because the output circuits are mirrored copies of each other, they should have identical properties including the more subtle features such as clock feedthrough. There are other benefits, such as the fact that the layout needs fewer cells and therefore is easier to check. A photograph of a completed device wafer on a 150-mm wafer is shown in Figure 2. The wafer holds six 2k×4k imagers plus smaller test imagers and process monitor structures around the perimeter.

Figure 3 provides details of the serial register layout and depicts the structure at the center point. The serial phase 3 (S3) runs the entire length of the register, and its gates are aligned to the parallel chanstops. Phases 1 and 2, however, are separated into left and right halves and brought out separately (S1A & S1B, S2A & S2B). These gates are aligned to the channels from the parallel section and would be clocked high during the parallel-serial transfer. This arrangement allows both bi- and uni-

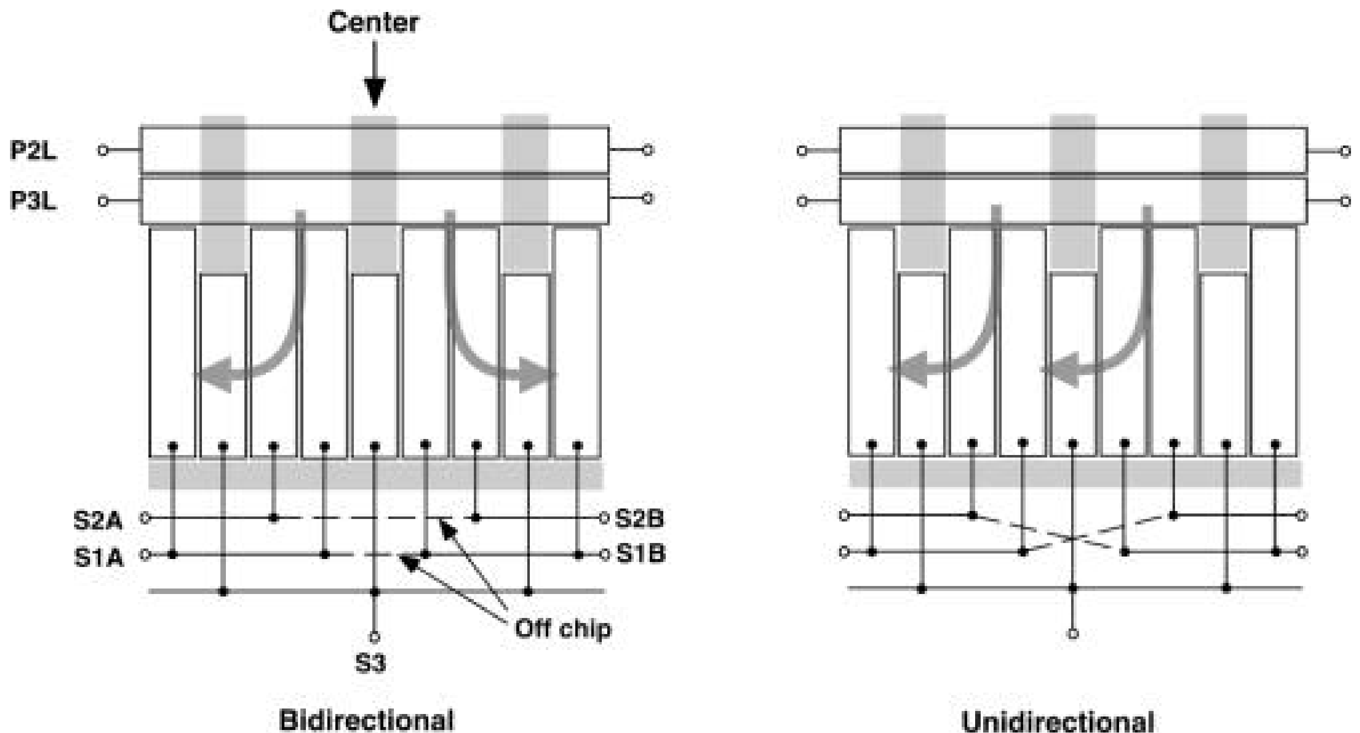


Figure 3. Details of parallel/serial interface at the center of the serial register.

A 2048×4096 CCD Imager for the U. of Hawaii Consortium

Barry E. Burke

Lincoln Laboratory, Massachusetts Institute of Technology
244 Wood Street
Lexington, Massachusetts 02420-9108
bburke@LL.MIT.EDU

Introduction

This document describes the design features of the 2048×4096, three-side-abuttable CCD imager developed by Lincoln Laboratory for the U. of Hawaii Consortium. We designate this device CCID-20 (Charge-Coupled Imaging Device #20). Beginning in early 1996 we fabricated several wafer lots of this device on 100-mm wafers. In late 1997 our wafer fab was converted to 150-mm wafers, and we have completed several lots of this device on the larger wafer size. This document briefly describes the main features of the device and its packaging.

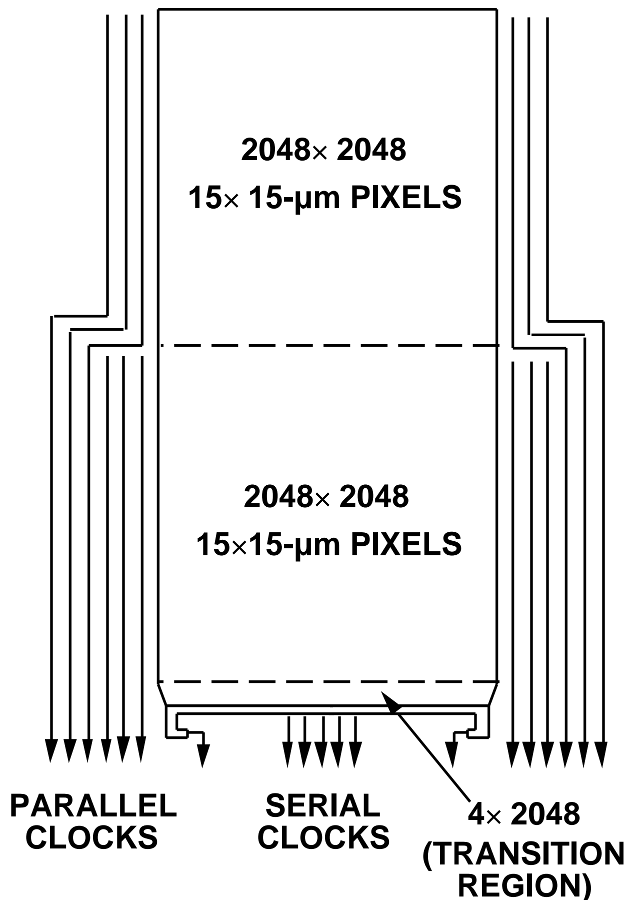


Figure 1. General layout of the imager.

Device Layout

Figure 1 depicts an overview of the device layout. This three-phase device is fabricated with a triple-poly, n-buried-channel process. Pixel size is 15×15 μm. The imaging section is segmented into two, independently clocked halves, so that frame-transfer operation is possible. There is, however, no interruption in the pixel layout across the boundary between the two sections, and therefore no image artifact of this division should be detectable. At the bottom of the lower half is a transition region of four rows, the purpose of which will be described later. The parallel clocks run down both left and right edges to provide some redundancy against metallization failure in these lines (which are somewhat narrow) and also to reduce the response time due of the gates to the clock waveforms. Excitation of the gates from both ends decreases the voltage rise and fall times on the gates by $4\times$ compared with single-ended excitation. A charge-collection diode, or "scupper," encircles the device and is used to help suppress spurious dark current and photocurrents from the edges of the device.