High-Speed, Low-Glitch D/CMOS Analog Switches

DESCRIPTION

The DG611/612/613 feature high-speed low-capacitance lateral DMOS switches. Charge injection has been minimized to optimize performance in fast sample-and-hold applications.

Each switch conducts equally well in both directions when on and blocks up to 16 V\textsubscript{pp} when off. Capacitances have been minimized to ensure fast switching and low-glitch energy. To achieve such fast and clean switching performance, the DG611/612/613 are built on the Vishay Siliconix proprietary D/CMOS process. This process combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. An epitaxial layer prevents latchup.

The DG611 and DG612 differ only in that they respond to opposite logic levels. The versatile DG613 has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, one DPDT.

For additional information see Applications Note AN207 (FaxBack number 70605).

FEATURES

- Fast Switching - \( t_{\text{ON}} \): 12 ns
- Low Charge Injection: ± 2 pC
- Wide Bandwidth: 500 MHz
- 5 V CMOS Logic Compatible
- Low \( r_{\text{DS(on)}} \): 18 Ω
- Low Quiescent Power : 1.2 nW
- Single Supply Operation

BENEFITS

- Improved Data Throughput
- Minimal Switching Transients
- Improved System Performance
- Easily Interfaced
- Low Insertion Loss
- Minimal Power Consumption

APPLICATIONS

- Fast Sample-and-Holds
- Synchronous Demodulators
- Pixel-Rate Video Switching
- Disk/Tape Drives
- DAC Deglitching
- Switched Capacitor Filters
- GaAs FET Drivers
- Satellite Receivers

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

![Functional Block Diagram and Pin Configuration](image)

TRUTH TABLE

<table>
<thead>
<tr>
<th>Logic</th>
<th>DG611</th>
<th>DG612</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>1</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>

Logic “0” ≤ 1 V
Logic “1” ≥ 4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply
DG611/612/613
Vishay Siliconix

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Four SPST Switches per Package

TRUTH TABLE

<table>
<thead>
<tr>
<th>Logic</th>
<th>SW1, SW4</th>
<th>SW2, SW3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>1</td>
<td>ON</td>
<td>OFF</td>
</tr>
</tbody>
</table>

Logic "0" ≤ 1 V
Logic "1" ≥ 4 V

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Temp Range</th>
<th>Package</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>- 40 to 85 °C</td>
<td>16-Pin Plastic DIP</td>
<td>DG611DJ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DG611DJ-E3</td>
</tr>
<tr>
<td></td>
<td>16-Pin Narrow SOIC</td>
<td>DG612DJ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DG612DJ-E3</td>
</tr>
<tr>
<td>DG611/612</td>
<td>16-Pin Plastic DIP</td>
<td>DG611DY</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DG611DY-E3</td>
</tr>
<tr>
<td></td>
<td>16-Pin Narrow SOIC</td>
<td>DG611DY-T1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DG611DY-T1-E3</td>
</tr>
<tr>
<td>DG613</td>
<td>16-Pin Plastic DIP</td>
<td>DG613DJ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DG613DJ-E3</td>
</tr>
<tr>
<td>- 40 to 85 °C</td>
<td>16-Pin Narrow SOIC</td>
<td>DG613DY</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DG613DY-E3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DG613DY-T1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DG613DY-T1-E3</td>
</tr>
</tbody>
</table>
## ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ to V-</td>
<td>- 0.3 to 21 V</td>
<td></td>
</tr>
<tr>
<td>V+ to GND</td>
<td>- 0.3 to 21 V</td>
<td></td>
</tr>
<tr>
<td>V- to GND</td>
<td>- 19 to 0.3 V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;L&lt;/sub&gt; to GND</td>
<td>- 1 to (V+) + 1 V or 20 mA, whichever occurs first</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IN&lt;/sub&gt;&lt;sup&gt;a&lt;/sup&gt;</td>
<td>(V-) - 1 to (V+) + 1 V or 20 mA, whichever occurs first</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;S&lt;/sub&gt;, V&lt;sub&gt;D&lt;/sub&gt;&lt;sup&gt;a&lt;/sup&gt;</td>
<td>(V-) - 0.3 to (V+) + 16 V or 20 mA, whichever occurs first</td>
<td></td>
</tr>
<tr>
<td>Continuous Current (Any Terminal)</td>
<td>± 30 mA</td>
<td></td>
</tr>
<tr>
<td>Current, S or D (Pulsed at 1 µs, 10 % Duty Cycle)</td>
<td>± 100 mA</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>CerDIP - 65 to 150 °C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Plastic - 65 to 125 °C</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation (Package)&lt;sup&gt;b&lt;/sup&gt;</td>
<td>16-Pin Plastic DIPC - 470 mW</td>
<td></td>
</tr>
<tr>
<td></td>
<td>16-Pin Narrow SOIC&lt;sup&gt;d&lt;/sup&gt; - 600 mW</td>
<td></td>
</tr>
<tr>
<td></td>
<td>16-Pin CerDIPC - 900 mW</td>
<td></td>
</tr>
<tr>
<td></td>
<td>20-Pin LCC&lt;sup&gt;e&lt;/sup&gt; - 900 mW</td>
<td></td>
</tr>
</tbody>
</table>

Notes:

a. Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings. 

b. All leads welded or soldered to PC Board.

c. Derate 6 mW/°C above 75 °C.

d. Derate 7.6 mW/°C above 75 °C.

e. Derate 12 mW/°C above 75 °C.

## RECOMMENDED OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limit</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+</td>
<td>5 to 21 V</td>
<td></td>
</tr>
<tr>
<td>V-</td>
<td>- 10 to 0 V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;L&lt;/sub&gt;</td>
<td>4 to V+</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>0 to V&lt;sub&gt;L&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;ANALOG&lt;/sub&gt;</td>
<td>V- to (V+) - 5</td>
<td></td>
</tr>
</tbody>
</table>

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### SPECIFICATIONS

#### Analog Switch
- **Analog Signal Range**
  - $V_{ANALOG} = -5 \, \text{V, } V_+ = 12 \, \text{V}$
- **Switch On-Resistance**
  - $r_{DS(on)} = -1 \, \text{mA, } V_D = 0 \, \text{V}$
- **Resistance Match Bet Ch.**
  - $\Delta r_{DS(on)}$
- **Source Off Leakage**
  - $I_{S(off)} = 0 \, \text{V, } V_D = 10 \, \text{V}$
- **Drain Off Leakage Current**
  - $I_{D(off)} = 10 \, \text{V, } V_D = 0 \, \text{V}$
- **Switch On Leakage Current**
  - $I_{D(on)} = 0 \, \text{V, } V_D = 0 \, \text{V}$

#### Digital Control
- **Input Voltage High**
  - $V_{IH}$
- **Input Voltage Low**
  - $V_{IL}$
- **Input Current**
  - $I_{IN}$
- **Input Capacitance**
  - $C_{IN}$

#### Dynamic Characteristics
- **Off State Input Capacitance**
  - $C_{S(off)} = V_S = 0 \, \text{V}$
- **Off State Output Capacitance**
  - $C_{D(off)} = V_D = 0 \, \text{V}$
- **On State Input Capacitance**
  - $C_{S(on)} = V_S = V_D = 0 \, \text{V}$
- **Bandwidth**
  - $BW = R_L = 50 \, \Omega$
- **Turn-On Time**
  - $t_{ON} = R_L = 300 \, \Omega, C_L = 3 \, \text{pF}$
- **Turn-Off Time**
  - $t_{OFF} = R_L = 300 \, \Omega, C_L = 75 \, \text{pF}$
- **Charge Injection**
  - $Q_{CL} = 1 \, \text{nF, } V_S = 0 \, \text{V}$
- **Ch. Injection Change**
  - $\Delta Q_{CL} = 1 \, \text{nF, } |V_S| \leq 3 \, \text{V}$
- **Off Isolation**
  - $OIRR_{IN} = 50 \, \Omega, R_L = 50 \, \Omega$
- **Crosstalk**
  - $X_{TALK} = R_{IN} = 10 \, \Omega, R_L = 50 \, \Omega$

#### Power Supplies
- **Positive Supply Current**
  - $I_+ = V_{IN} = 0 \, \text{V or } 5 \, \text{V}$
- **Negative Supply Current**
  - $I_- = V_{IN} = 0 \, \text{V or } 5 \, \text{V}$
- **Logic Supply Current**
  - $I_L$
- **Ground Current**
  - $I_{GND}$

---

**Note:**
- Symbol: $V_+$ or $V_-$
- Test Conditions: $V_+ = 15 \, \text{V, } V_- = -3 \, \text{V}$
- Temp: $-55$ to $125 \, ^\circ\text{C}$, $-40$ to $85 \, ^\circ\text{C}$

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**DG611/612/613**

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### SPECIFICATIONS FOR UNIPOLAR SUPPLIES

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions Unless Otherwise Specified</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$V_+ = 15, \text{V}$, $V_- = -3, \text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_L = 5, \text{V}$, $V_{\text{IH}} = 4, \text{V}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Temp $^b$</th>
<th>Typ $^c$</th>
<th>Min $^d$</th>
<th>Max $^d$</th>
<th>Min $^d$</th>
<th>Max $^d$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Switch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Signal Range $^a$</td>
<td>$V_{\text{ANALOG}}$</td>
<td>Full</td>
<td>0</td>
<td>7</td>
<td>0</td>
<td>7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Switch On-Resistance</td>
<td>$r_{\text{DS(on)}}$</td>
<td>Room</td>
<td>25</td>
<td>60</td>
<td>60</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

**Dynamic Characteristics**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn-On Time $^a$</td>
<td>$t_{\text{ON}}$</td>
<td>$R_L = 300, \Omega$, $C_L = 3, \text{pF}$, $V_S = 2, \text{V}$, See Test Circuit, Figure 2</td>
</tr>
<tr>
<td>Turn-Off Time $^a$</td>
<td>$t_{\text{OFF}}$</td>
<td>Room</td>
</tr>
</tbody>
</table>

### Notes:

a. Refer to PROCESS OPTION FLOWCHART.
b. Room = $25\, ^\circ\text{C}$, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
e. Guaranteed by design, not subject to production test.
f. $V_{\text{IN}} = $ input voltage to perform proper function.
g. $\Delta Q = |Q$ at $V_S = 3\, \text{V} - Q$ at $V_S = -3\, \text{V}|$

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS

25 °C, unless otherwise noted

---

**r_{\text{DS(on)}} vs. V_D and Power Supply Voltages**

**Leakage Current vs. Analog Voltage**
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

- Input Switching Threshold vs. \( V_L \)
- \( r_{DS(on)} \) vs. \( V_D \) and Temperature
- Leakage Currents vs. Temperature
- Switching Times vs. Temperature
- Charge Injection vs. Analog Voltage
- \(-3\) dB Bandwidth/Insertion Loss vs. Frequency
TYPICAL CHARACTERISTICS  25 °C, unless otherwise noted

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

TEST CIRCUITS

Figure 1.

Figure 2. Switching Time
APPLICATIONS

High-Speed Sample-and-Hold

In a fast sample-and-hold application, the analog switch characteristics are critical. A fast switch reduces aperture uncertainty. A low charge injection eliminates offset (step) errors. A low leakage reduces droop errors. The CLC111, a fast input buffer, helps to shorten acquisition and settling times. A low leakage, low dielectric absorption hold capacitor must be used. Polycarbonate, polystyrene and polypropylene are good choices. The JFET output buffer reduces droop due to its low input bias current. (See Figure 5.)

Pixel-Rate Switch

Windows, picture-in-picture, title overlays are economically generated using a high-speed analog switch such as the DG613. For this application the two video sources must be sync locked. The glitch-less analog switch eliminates halos. (See Figure 6.)

GaAs FET Drivers

Figure 7 illustrates a high-speed GaAs FET driver. To turn the GaAs FET on 0 V are applied to its gate via S1, whereas to turn it off, - 8 V are applied via S2. This high-speed, low-power driver is especially suited for applications that require a large number of RF switches, such as phased array radars.

![Figure 3. Charge Injection](image1)

![Figure 4. Crosstalk](image2)

![Figure 5. High-Speed Sample-and-Hold](image3)
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