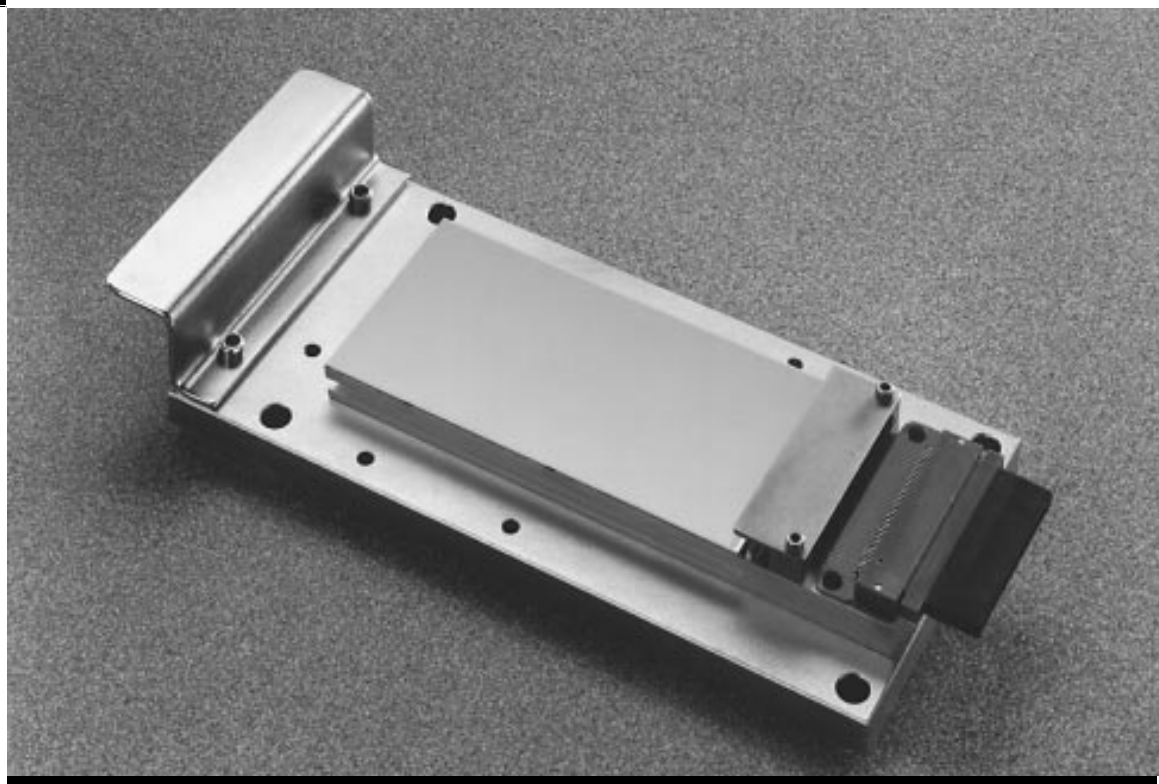

PRELIMINARY

SITe 2048 x 4096 Scientific-Grade CCD

ST-002A CCD Imager: *Ideal for Astronomy, Spectroscopy, and Time-Delayed Integration applications*

- 2048 x 4096 pixel format (15μm square)
- Front-illuminated or thinned, back-illuminated versions
- Three side buttability to facilitate large mosaic focal planes
- Special packaging to facilitate mosaic layouts
- Frame Transfer Architecture with imaging and memory regions
- Excellent QE from IR to UV
- MPP technology
- Low dark current
- Excellent charge transfer efficiency (CTE) at all signal levels
- On-chip, low noise output MOSFETs designed for high dynamic range
- Applications include astronomy, spectroscopy, medical imaging, X-ray imaging, and scientific imaging

General Description

The SITe ST-002A CCD Imager is a silicon charge-coupled device designed for imaging applications requiring a large focal plane. Three side buttability and special packaging to facilitate close placement of the arrays with minimal image loss in the interstices provide the capability to array numerous devices. The frame transfer architecture provides the ability to capture and store images rapidly, and the split serial readout register along the shorter dimension maximizes readout flexibility. The capability to read simultaneously from two outputs also enhances the image processing time. These features provide significantly enhanced capabilities in astronomy, medical X-ray imaging, and spectroscopy applications. The capability to array imagers to cover large areas is especially useful for full breast mammography X-ray imaging and the increasingly large focal planes of new generation telescopes.

Time-Delayed Integration where the image is scanned across the imager in synchronism with the parallel clocking rate can be utilized to enhance the signal to noise of the imager and improve the quality of the image or the spectra being studied.

The ability to image over a wide spectral range from IR to UV, the enhanced quantum efficiency over this wide range of spectral wavelengths, and the low noise of ST-002A are very attractive features. The ST-002A is a three phase, frame transfer device with a 100% optical fill factor, so the maximum area of the sensor is actively gathering the image or the dispersed light spectra. The device also features a buried channel with a minichannel for high transfer efficiency at low signal levels which is very important when attempting to analyze weak

images and spectral lines. Multi-phase pinned (MPP) operation for low dark current and a lightly doped drain output MOSFET for low read noise enhance the detection of weak images or spectra. The imager is available in a front illuminated version and a thinned, back-illuminated version which is the unique SITe technology that the provides superior quantum efficiency over a wide range of wavelengths from near IR to UV.

Functional Description

Imaging Area

As shown in the functional diagram, Figure 4, the imaging area of the ST-002A consists of 2048 columns, each of which contains 4096 picture elements (pixels). Each pixel measures 15μm x 15μm. The columns are isolated from each other by channel-stop regions. The 2048 columns are divided into two sections of 2048 rows each (upper and lower sections). The 4096 rows of pixels are further divided into two groups of 1024 columns (A and B sections) for clocking flexibility and output amplifier selection. There are 25 additional extended pixels on each side of the serial readout register just before the A and B output amplifiers. The parallel columns can be clocked in such a manner as to perform a frame transfer of the upper 2048 x 2048 pixels into the lower 2048 x 2048 pixels which can serve as an image memory buffer. This buffer can be read out while the upper image region of the array collects another image. By shutting off the P3U clocks, the upper region of the array can collect a new image (integrate) while the P3L clocks shift out the previously acquired image. At the top of the array, an overflow drain limits the amount of charge blooming of bright image spots into the serial register. It also serves to capture stray charge generated in the substrate regions.

The signal charge collected in the imaging array is transferred along the columns, one row at a time, to the serial output register and from there to the two output amplifiers.

Three levels of polysilicon are used to fabricate the three gate electrodes which form the basic CCD cell or pixel. All of the pixels in a given row are defined by the same three gates. Corresponding gates in each row within a group of phase one (P1) or phase two (P2) are connected in parallel at both edges of the array. Phase three (P3) of the upper and lower sections are independently bussed in parallel and brought out individually in order to clock the array in the frame transfer mode of operation. The clock signals used to drive the imaging area gates are brought in from both edges of the array, thus increasing the rate at which the rows can be shifted.

Serial Registers

The entire array is readout through one serial output register which allows additional arrays to be mounted adjacent to each other on three sides (buttability) with a minimum amount of lost imaging area at the seams. Seam width between devices is approximately 700μm along the sides and 350μm at the top.

The functional diagram (Figure 4) illustrates the relationship between the imaging array and the serial register. The charge collected in the lower memory section is transferred into the serial register phase 1 gate. The serial register has one pixel for each column in the imaging array, plus 25 extra pixels at each end for a total of 2098 serial pixels. The extra pixels serve as dark reference and ensure that the signal chain is stabilized when the image data is received at the output. The serial register accommodates double the full well charge of an individual parallel array pixel.

Each end of the output serial register terminates in a summing well, a DC-biased last gate (which serves to decouple the serial clock pulses from the output node), and an output amplifier. The summing well is a separately clocked gate equal in charge capacity to the other serial gates. It can be used to provide on-chip (noiseless) charge summing of consecutive serial pixels. Similarly, it is possible to sum pixels into the serial register by performing repetitive parallel transfers with the serial clocks stopped. In this manner, it is possible to collect and detect as one large pixel the sum of the charge in sub-arrays of the imaging section -- provided that the sum of the charge is less than the full well charge of the serial pixel. The well capacity of a pixel in the serial register is 2X greater than that of a parallel pixel to ensure that the dynamic range is not limited by the serial register.

The two sections of the serial register are bussed separately for phases 2 and 3, but the phase 1 pins within the serial register are internally connected (thus labeled S1ab). The serial register can be clocked such that both amplifiers can be read out individually or simultaneously. Thus, the array can be divided into two halves for maximum data transfer rate. The two halves are designated by the letters A and B, corresponding to the nearest output amplifier.

This architecture permits images to be read out in a variety of ways. The readout options are represented in the CCD timing diagrams and are described in a later section.

Output Structure

The imager has two output MOSFETs located at bottom of the array at the ends of the extended serial register. Figure 1 presents a schematic diagram of the output configuration.

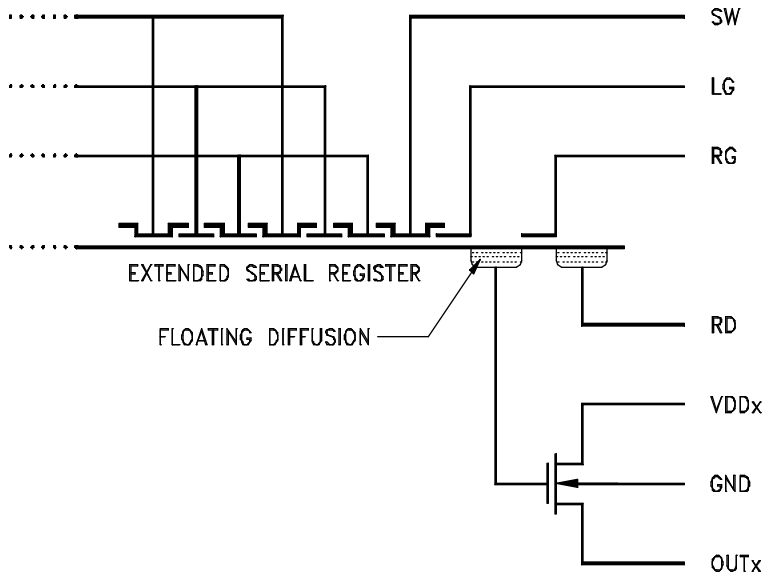

FIGURE 1 *Output Structure*

In operation, a positive pulse is applied to the reset gate which sets the potential of the floating diffusion to the potential applied to the reset transistor drain (RDx). The reset gate voltage is then turned off and the output node (the floating diffusion) is isolated from the rest of the circuit. Charge from a serial pixel is then transferred to the output node on the falling edge of the summing well (SWx) clock pulse. The addition of charge on the output node causes a change in the voltage on the gate of the output MOSFET. This voltage change is sensed at OUTx.

Timing

The SITe ST-002A CCD Imager may be operated with one or two outputs operating simultaneously. The serial gates are separated into left and right halves. Similarly, the parallel gates are separated into upper and lower halves. The partitions formed are designated as upper gates (image), lower gates (memory), output A (lower left), and output B (lower right). See Figure 4.

When operated in the full frame mode, the entire imager's signal is transferred to one output, and all of the same numbered phases of the serial register are clocked together. For example, Serial phases S2a and S2b plus S3a and S3b would be wired together. Likewise P3U and P3L would be wired and clocked together. P1 and P2 for the upper and lower sections are always bussed and clocked together. The signal charge may be clocked out of either A or B outputs; however, the timing must be appropriately selected for that output.

The ST-002A may also be operated in the dual output mode where the signal charge is clocked out of two outputs simultaneously. The charge in each array half is transferred to the nearest output. The serial gates in each half are applied clocking signals appropriate for full frame operation of that output. For example, S2a, S3a and SWa would be clocked according to OUTa timing, and S2b, S3b and SWb would be clocked according to OUTb timing. Note: S1ab of the serial register is internally connected and should be driven by a common clock driver. The parallels would be operated the same for full-frame operation with either OUTa or OUTb. Timing diagrams for both outputs are shown in Figure 5. During a parallel or serial shift, the signal charge is transferred one pixel. A frame readout consists of at least 4096 parallel shift/serial readout sequences for full frame and 2048 for split parallels reading out just the lower half or memory section. Figure 6 shows the typical timing for a full frame readout. A serial readout sequence consists of at least 2098 serial shifts for full frame mode (50 for the serial extended regions plus 2048 pixels of data from the imaging array); 1049 (1024+25) for split serial modes. The serials are static when the parallels are shifting and vice-versa. During integration, the serial clocks can be kept running continuously to flush the serial registers and to stabilize the bias levels in the off-chip signal chain. Alternately, apply a DC bias to all the serial gates and then clock 1 or 2 lines to stabilize the signal chain before beginning read out.

The timing diagrams (Figures 5 and 6) are for integration under parallel phases 1 and 2. For MPP operation, this timing is a requirement (as it is with all SITe MPP devices). For non-MPP operation this is also a desirable option, since the number of rows will remain the same as for MPP operation.

Multi-Phase Pinned (MPP) Operation

The multi-phase pinned (MPP) technology used on the ST-002A allows the device to be operated totally inverted during integration and line readout. The main advantage of this mode of operation is that it results in much lower dark current than conventional CCD operation. Other advantages of MPP operation are the reduction of surface residual image effects and a greater tolerance for ionizing radiation environments.

To operate the CCD in the MPP mode, the array clocks are biased sufficiently negative to invert the n-buried channel and "pin" the surface potential beneath each phase to substrate potential. This allows holes from the p+ channel stop to populate the surface states at the silicon/silicon dioxide interface which minimizes surface dark current generation.

To enable all three phases of the array to be inverted and still retain well capacity, MPP devices have an extra implant under the phase 3 gates. During integration, this creates a potential barrier between each pixel allowing signal charge to accumulate under phase 1 and 2 at each pixel site. A consequence of this mode of operation is that the total well capacity is about 50 percent of that of a standard CCD, if all the parallel clocks are operated at the same voltages. A larger well capacity can be obtained if phase 3 parallel clock high rail is operated about 3 volts higher than the phase 1 and phase 2 high rails.

DEVICE SPECIFICATIONS

Unless otherwise indicated, all measurements are made at standard conditions of -80°C, 45 kpixels/second, using a dual slope CDS with 8 μsec integration time.

FORMAT	Frame-Transfer, 4096 X 2048 pixels		
PIXEL SIZE	15μm x 15μm		
IMAGE AREA	30.72mm x 30.72mm		
MEMORY AREA	30.72mm x 30.72mm		
DIE SIZE	63.43mm x 31.46mm		
PARAMETER	**MIN, MAX OR TYPICAL.**		**UNITS**
		GRADE 1, 2	
MPP Dark Current (20C ref.)	typical	30	pA/cm^2
	max	100	pA/cm^2
Non-MPP Dark Current (20C ref.)	typical	100	pA/cm^2
	max	500	pA/cm^2
Readout Noise	typical	2-4	electrons, rms
	max	7	electrons, rms
Parallel Full Well	typical	100,000	electrons
	min	60,000	electrons
Serial Full Well	typical	200,000	electrons
	min	120,000	electrons
Serial readout clock rate	typical	45	KHz
	max	2-4	MHz
Amplifier Gain	typical	1.8	μV/electron
	min	1.2	μV/electron
CTE	min	0.99995	@ 500 electrons
		0.99999	@ 5000 electrons
Flatness	typical	TBD	μm
Dead region between devices:			
-----seam width along the sides	by design	697	μm
-----seam width along the top	by design	325	μm
-----max. tolerances	by manufacture	TBD	
QE	see QE curve FIGURE 7		

TABLE 1 ST-002A *Device specifications*

DC OPERATING CONDITIONS

TERMINAL	ITEM	MIN	STANDARD	MAX	UNIT
VDDx	OUTPUT DRAIN SUPPLY	21	24.3	26	V
RDx	RESET DRAIN SUPPLY	12	14	16	V
LGx	LAST GATE	-5	-4	0	V
SUB, PKG	SUB & PACKAGE CONNECTION	-10	0	10	V
GNDx	MOSFET GROUND REFERENCE	-10	0	10	V
OUTx	MOSFET OUTPUT (LOAD)	5	20	50	kohms

GATE TO SUBSTRATE VOLTAGES

TERMINAL	ITEM	MIN	STANDARD	MAX	P TO P MAX	UNIT
RGx	RESET GATE				20	V
	LOW RAIL	-5	0	5		V
	HIGH RAIL	7	12	20		V
S#x	SERIAL GATE				20	V
	LOW RAIL	-12	-7	0		V
	HIGH RAIL	5	5	15		V
SWx	SUM WELL				20	V
	LOW RAIL	-10	-6	0		V
	HIGH RAIL	5	5	15		V
P#x	PARALLEL GATE				20	V
	LOW RAIL	-12	-10	0		V
	HIGH RAIL	0	2	15		V
P3	HIGH RAIL	0	7	15		V
	LOW RAIL	-10	-8	0		V
	HIGH RAIL	0	5	15		V

TABLE 2 ST-002A *DC operating conditions and clock voltages*

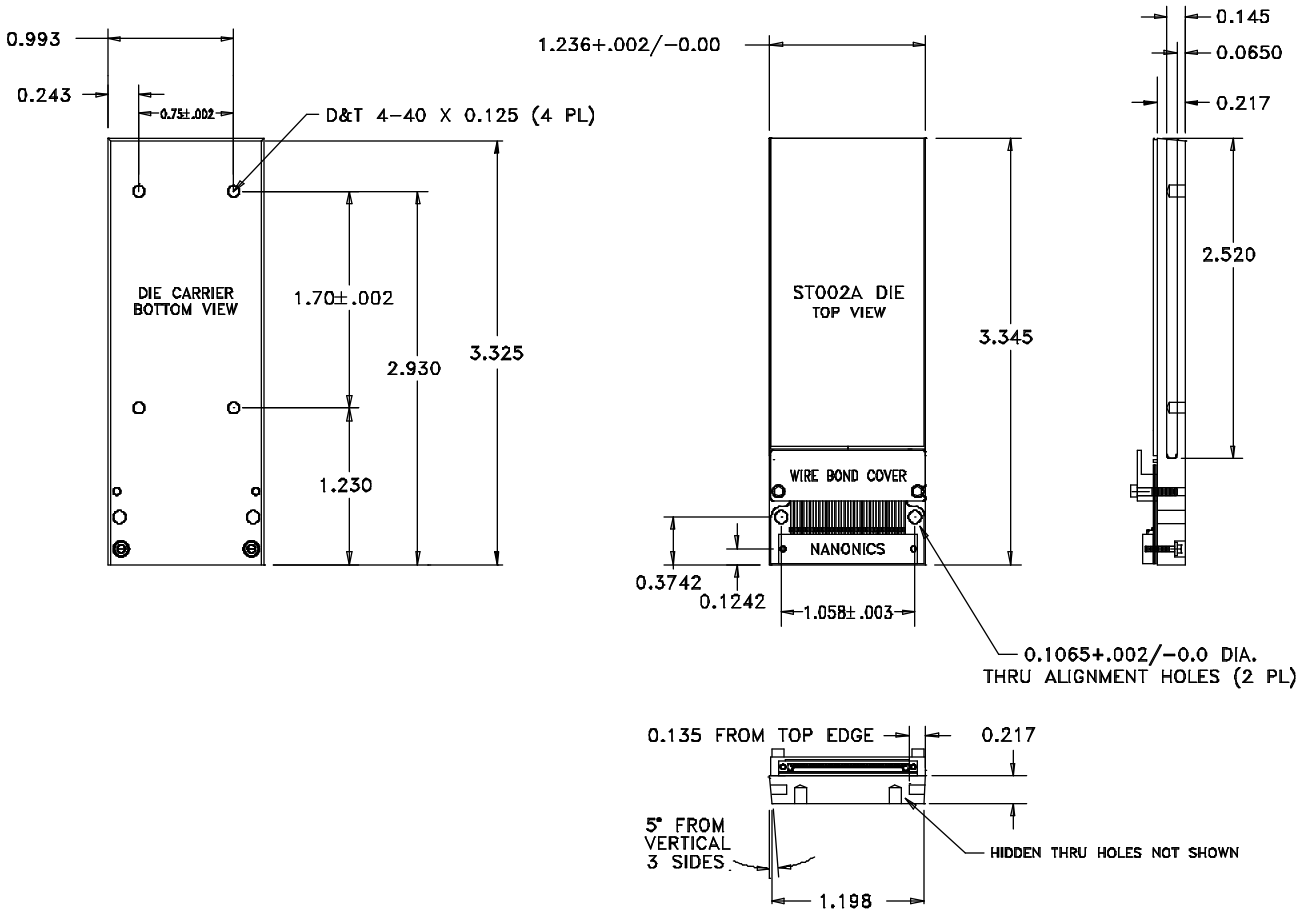

FIGURE 2 ST-002A *package configuration*

NANONICS PIN OUT	FUNCTION AT NANONICS PIN OUT	SYMBOL	NANONICS PIN OUT	FUNCTION AT NANONICS PIN OUT	SYMBOL
1	A output reset transistor gate	RGa	20	Chip Temp. Sense Diode (+)	CHIP TSD+
2	A output reset transistor drain	RDa	21	CHIP GROUND	CHIP GND
3	A output transistor drain	VDDa	22	Overflow drain	OFD
4	A output transistor source	OUTa	23	Parallel phase 1	P1
5	Last gate, A output	LGa	24	Parallel phase 2	P2
6	Package Ground	GND	25	Parallel phase 3, lower register	P3L
7	Sum well, A output	SWa	26	Parallel phase 3, upper register	P3U
8	GROUND	GND	27	Serial phase 1, AB register	S1ab
9	Serial phase 3, A register	S3a	28	Serial phase 2, B register	S2b
10	Serial phase 2, A register	S2a	29	Serial phase 3, B register	S3b
11	Serial phase 1, AB register	S1ab	30	GROUND	GND
12	Parallel phase 3, upper register	P3U	31	Sum well, B output	SWb
13	Parallel phase 3, lower register	P3L	32	GROUND	GND
14	Parallel phase 2	P2	33	Last gate, B output	LGb
15	Parallel phase 1	P1	34	B output transistor source	OUTb
16	Overflow drain	OFD	35	B output transistor drain	VDDb
17	CHIP GROUND	CHIP GND	36	B output reset transistor drain	RDb
18	AD590 Temp. Sense Diode (+)	AD590 TSD+	37	B output reset transistor gate	RGb
19	Common Temp. Sense Diode (-)	COM TSD-			

TABLE 3 ST-002A *pin definitions for front and back illuminated devices*

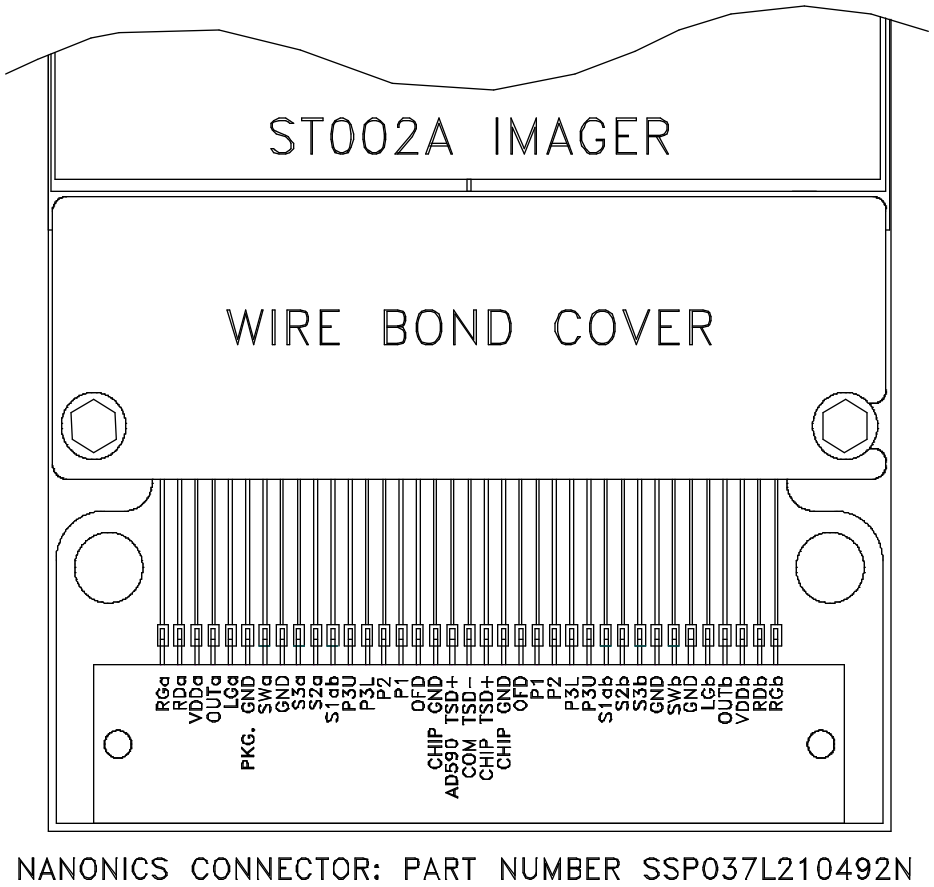

FIGURE 3 ST-002A *Front and Back illuminated device pin labels (as viewed from top of package)*

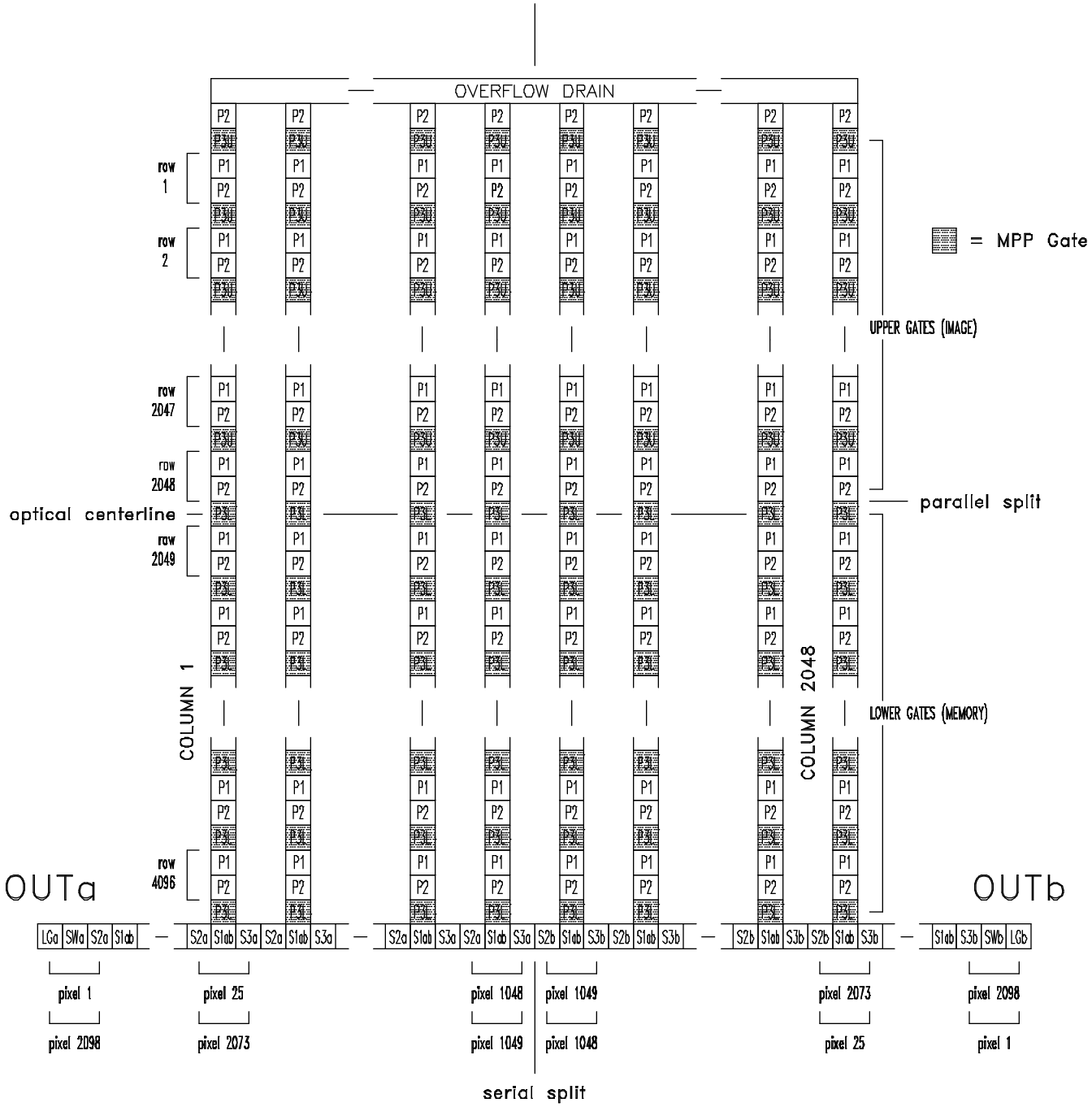

FIGURE 4 ST-002A *functional diagram*

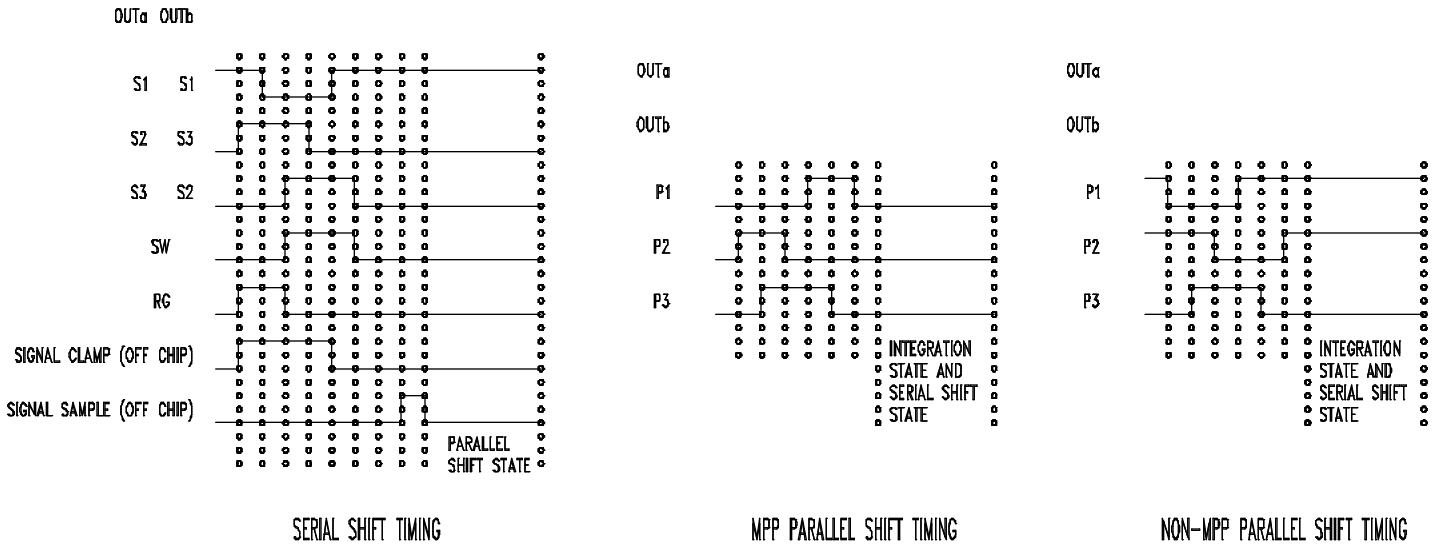

FIGURE 5 *Serial and Parallel timing for both outputs*

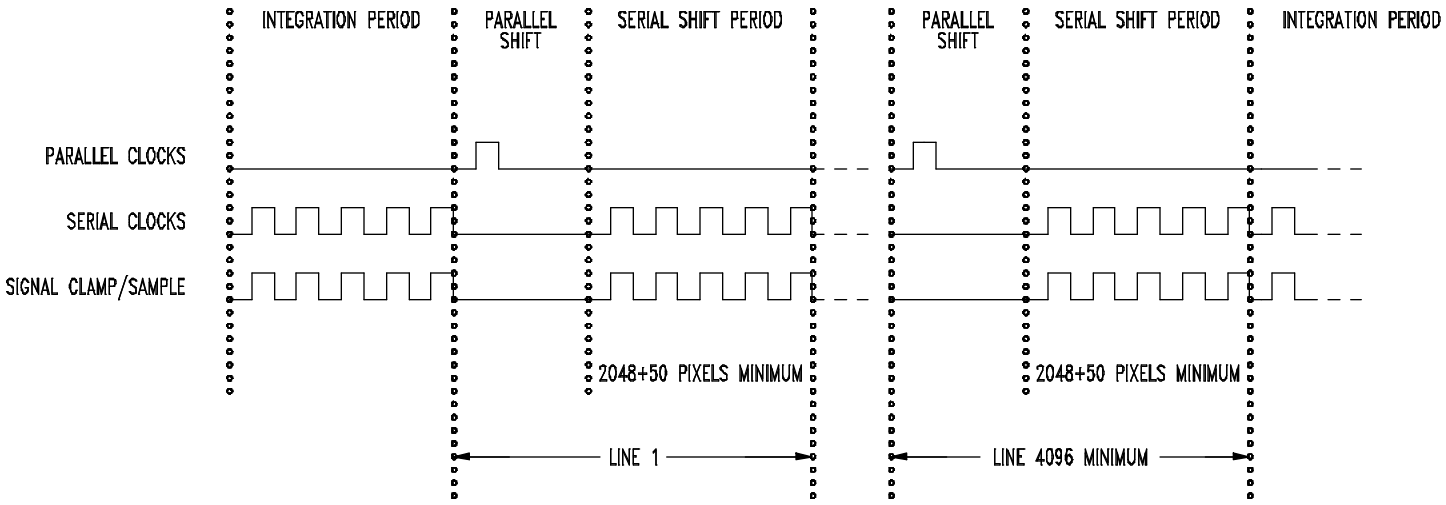

FIGURE 6 *Typical full-frame readout*

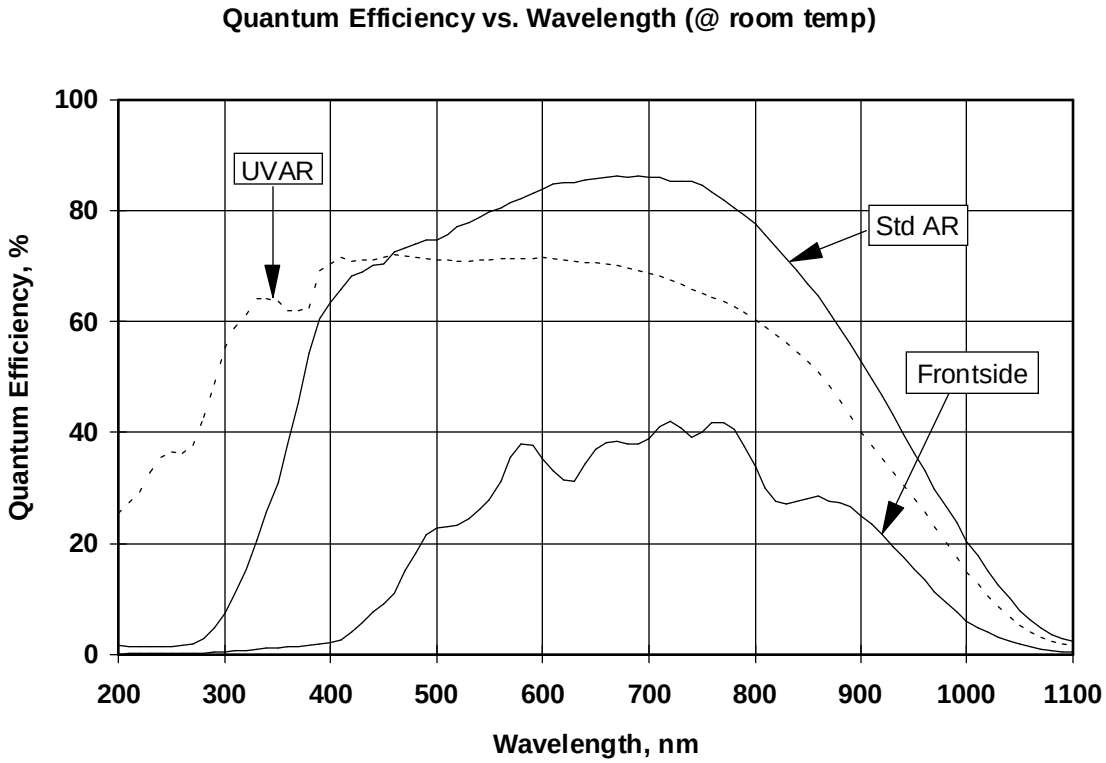

FIGURE 7 *Typical QE curves*

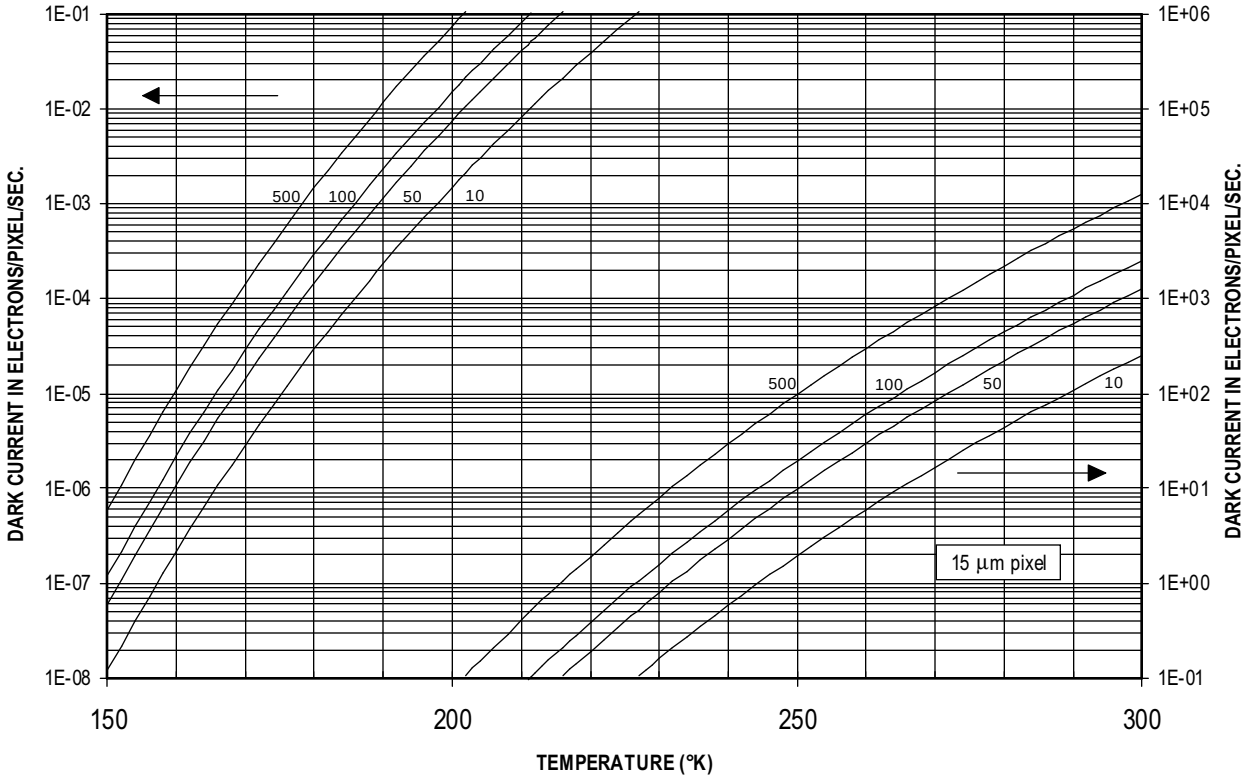

FIGURE 8 *Effect of temperature on dark current. Parameter is pAmp/cm^2 at 293K*

SCIENTIFIC IMAGING TECHNOLOGIES, INC.

P.O. Box 569
Beaverton, Oregon 97075-0569
503/644-0688
503/644-0798 fax

Scientific Imaging Technologies, Inc. (SITe) specializes in the research, design, and manufacture of charge-coupled devices (CCDs) and imaging subassemblies containing CCD components. SITe's scientific grade CCDs are used in applications for astronomy, aerospace, medical, military surveillance, spectroscopy, and other areas of imaging research. Commercial uses of SITe high performance CCDs include such areas as biomedical imaging, manufacturing quality control, environmental monitoring, and nondestructive testing.

With its focus on scientific-grade CCD imaging components and modules, SITe provides standard designs, user defined custom CCDs, and foundry services. SITe's engineering and manufacturing team builds custom CCD imagers for use in the most demanding applications including NASA programs, satellite platforms, and other research projects. Device formats are available as front illuminated or thinned, back illuminated CCDs.

Innovation, process development, and design experience date back to the founding of the group in 1974.

Product Precautions

Scientific Imaging Technologies, Inc. (SITe) realizes the use of charge-coupled devices (CCDs) for imaging is rapidly expanding into new applications. Awareness of the sensitivity of CCDs to electrostatic discharge (ESD) damage and the steps that can be implemented to prevent damage are very important to the end user.

With the exception of the back-illuminated SI424A, SITe imagers do not have built-in gate protection structures. Even with the protection structures, the imagers are very sensitive to ESD damage. It is imperative that proper precautions be taken whenever the imagers are handled.

The damage caused by ESD can be immediate and fatal (hard damage) resulting in a completely nonfunctional device. ESD damage can also be more subtle with no immediate device performance degradation. In this case, the result is a slow deterioration (soft damage) that may not be apparent until after extended operation.

There are three major areas where special procedures are required. We recommend that our customers use these procedures to minimize the risk of ESD damage.

1. Work areas specifically designed to minimize ESD.

2. Personnel requirements for ESD damage protection.

3. Use special ESD protected handling and shipping containers. SITe has developed a custom shipping container which grounds all the CCD pins together and allows clean and safe handling for incoming inspection and storage.

For more specific information on minimizing ESD damage, refer to SITe's technical briefing called "Recommended ESD Handling Procedures For CCD Imagers."

SITe Lit. No. ST-002A,
version date: 12/21/95