

HAWAII-2RG

Technical Manual



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1 General Overview

The HAWAII-2RG (HgCdTe Astronomy Wide Area Infrared Imager with 2K x 2K resolution, Reference pixels and Guide mode) multiplexer has been designed to operate in a number of different operation modes allowing the user to adapt the performance to the specific application. Lowest read noise is achieved at the 100 kHz “slow” data rate, while a high speed mode gives a “fast” data rates of up to 5 MHz combined with programmable gain at the cost of slightly increased (~x5) read noise. Up to 32 parallel outputs provide high frame rates while the single output mode features the lowest power consumption at less than 0.5 mW. An integrated window mode allows instant random access to any rectangular-shaped subarray. For guide mode operation, full field and window readout can be combined in order to simultaneously facilitate long science integration and fast guide window readout. Additional reference pixels track voltage drifts caused by temperature or bias voltage variations. They enable an immediate compensation during readout using the extra reference output as well as a detailed offline analysis using the reference information embedded in the regular data stream.

A basic overview of the multiplexer layout can be seen in Figure 1-1. It shows the 2048 x 2048 pixel array in the center, the vertical scanner to the left, the horizontal scanner and the column buffers (for high speed readout) at the top, the clock buffers and storage registers in the upper left corner and the row of I/O Pads at the very top. The horizontal and vertical scanners consist of two parts: a main shift register for the full field readout and a second shift register plus decoder for the window readout. Both registers in each scanner are controlled by the same set of clocks which, depending on the selected mode, control either the full field or the window mode shift registers. The readout has been designed with the I/O pads only along the top edge of the readout, providing three sides with close buttability and the fourth (top) side with near buttability.

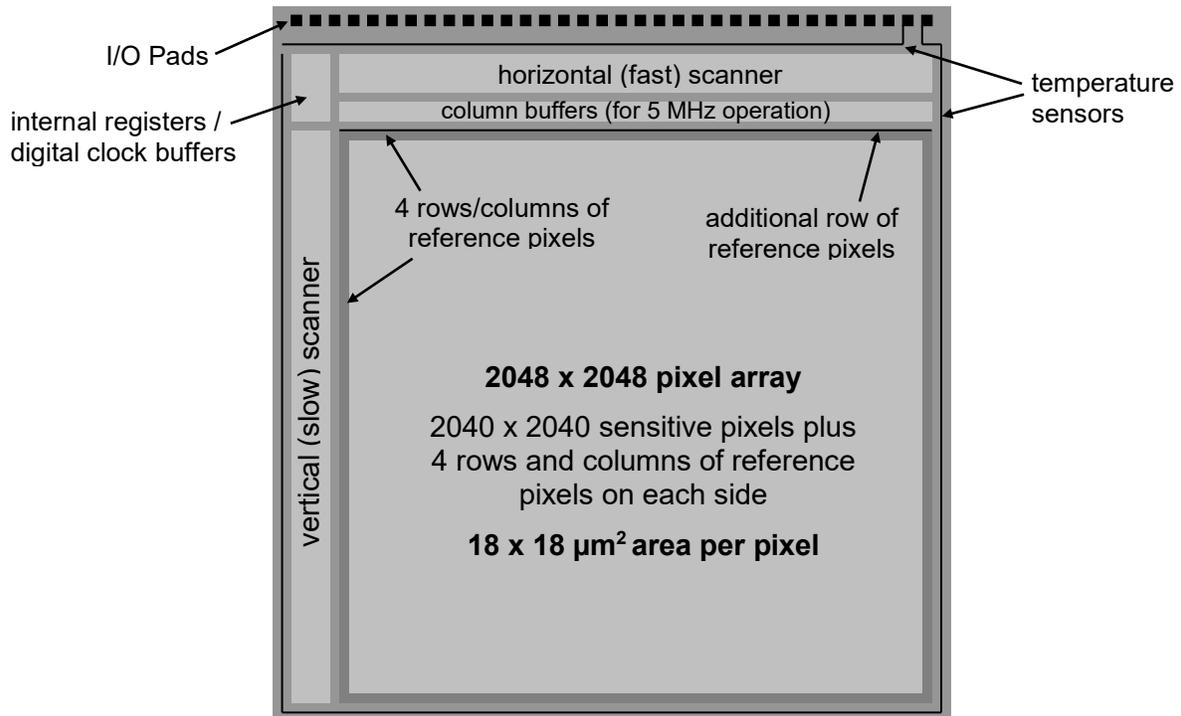


Figure 1-1: Block diagram of the HAWAII-2RG

The pixel array itself is surrounded by 4 rows and columns of reference pixels included in the array of 2048 x 2048 pixels. Therefore, the active area consists of 2040 x 2040 light sensitive pixels. An additional row of reference pixels with alternating capacitance values can be found at the top of the array. It can be used for evaluation and diagnostic purposes, but is disabled during the normal readout operation. Two temperature sensors, one at the top of the array and one along the other three sides of the array, allow the user to monitor the FPA temperature by measuring the resistance change in either of these long metal lines.

The unit cell (pixel) consists of seven transistors and is optimized for low noise and high dynamic range readout and single pixel reset operation. Its principal architecture is shown in Figure 1-2. To allow single pixel reset both a horizontal and a vertical line control the reset switch. The switch is closed only if both control lines are enabled. By this means, a single pixel can perform the reset without influencing the other pixels in the same row or column. The active detector (photo diode) is bump bonded to the multiplexer unit cell. When the pixel is selected for read by the Read Control Line, the detector voltage at the integrating node is buffered by the unit cell output transistor and read out through the Vertical Read Bus.

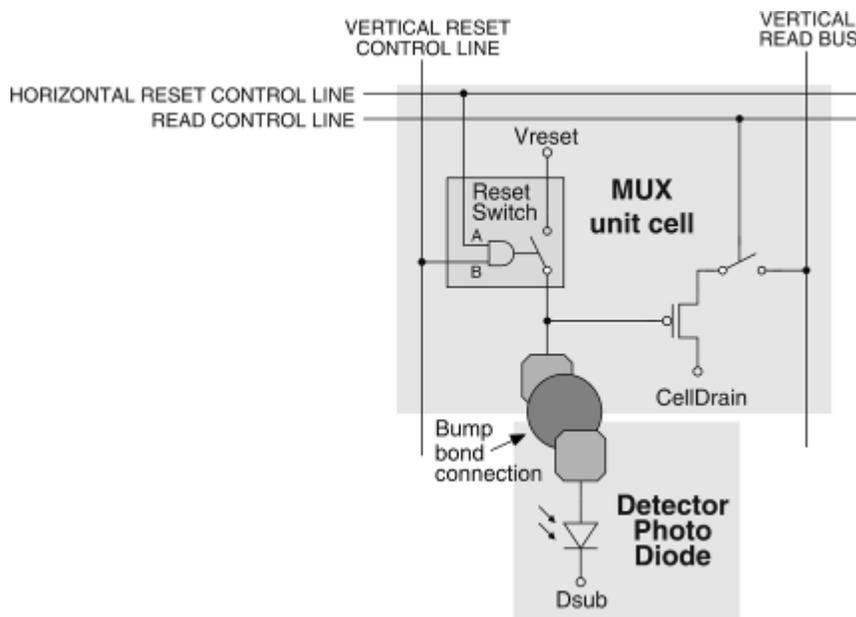


Figure 1-2: Architecture of the HAWAII-2RG unit cell (pixel)

The HAWAII-2RG multiplexer has been realized in a 0.25 μm CMOS process that, due to the low gate oxide thickness, offers a high intrinsic radiation hardness. In addition, the vertical shift register and the internal mode registers are immune to single event upsets (SEU). This ensures that the multiplexer does not accidentally switch to another operation mode or read two rows at a time. Because there is a power penalty for the SEU proof latches, the horizontal scanner is composed of standard latches. Here, the clock frequency is much higher and a single bit upset, in worst case, destroys a single row but not the whole frame.

2 Input/Output signals and requirements

The HAWAII-2RG multiplexer has a total of 124 I/O pads all of which are located in a single straight line along the top side of the focal plane array. However, only a subset of I/O signals is needed for a particular operation or output mode. The simplest readout operation, for example, requires only 18 I/O pads (100 kHz readout speed, single output). Depending on the additional user required features, other or more I/O signals will be needed. The following sections describe the individual pads in detail. An overview of all I/O signals can be found in Table A.1 on page 49.

2.1 Power Supply

gnd: Digital ground (0 V). It supplies the power return for the horizontal and vertical scanner logic, the clock buffers, and the serial interface logic.

vdd: Digital positive power supply ($3.3\text{ V} \pm 5\%$). It supplies the power for the horizontal and vertical scanner logic, the clock buffers, and the serial interface logic. Overall power consumption is small ($< 10\ \mu\text{A}$ for 100 kHz operation), however short spikes requiring several mA can occur. Therefore, an external capacitive blocking to gnd is essential with $C \geq 100\ \text{nF}$.

gnda: Analog ground (0 V). It supplies the power return for the internal analog components like the protection diodes, n-well, sample&hold stage, column buffer, and 5 MHz output buffer.

vdda: Analog positive power supply ($3.3\text{ V} \pm 5\%$). It supplies the power for the internal analog components like the protection diodes, n-well, sample&hold stage, column buffer, and 5 MHz output buffer. During 100 kHz operation, no current is drawn. During 5 MHz operation, the total current per output channel is about 0.6 mA plus an additional 0.5 mA if the output buffer is enabled. For noise reduction purposes, vdda should be capacitively blocked to gnda with $C \geq 100\ \text{nF}$.

sub: Multiplexer substrate (0 V). This must be the lowest voltage on the multiplexer. It can be externally connected to gnda.

Celldrain: Drain node of the pixel source follower (0 V or more). In 100 kHz mode, the consumed current is approx. $20\ \mu\text{A}$ per output channel (and twice the amount of current in a single active unit cell source follower). In 5 MHz mode, the current rises to a total of about 5 mA independent of the selected output mode. The exact current depends on the bias voltage V_{biasgate} which controls the source follower current source. In any mode, an external blocking capacitor to gnda with $C \geq 100\ \text{nF}$ should be used. To reduce the on-chip power consumption, Celldrain can be set slightly higher than 0 V; however, it must not exceed the lowest possible detector voltage, D_{sub} or V_{reset} , whichever is lower. Externally, Celldrain can be directly connected to gnda if on-chip power consumption at 0 V is acceptable or minimum I/O line count is critical.

Drain: Drain node of the output source follower (0 V or more). Only used in 100 kHz mode if the output buffer is enabled (see BUFFERDISABLE in Section 2.4). The consumed current depends on the externally applied load resistor or current source. In order to reduce the on-chip power consumption, Drain can be slightly increased above 0 V; however, it must stay lower than the lowest detector voltage + 800 mV. For example, if the detector reset voltage V_{reset} is 0 V ($D_{\text{sub}} > 0\ \text{V}$), Drain cannot exceed 800 mV in order to prevent non-linearities in the transfer characteristics. Drain should be either directly connected to or capacitively blocked to gnda with $C \geq 100\ \text{nF}$.

Vbiaspower: Source node of the internal current source for the pixel source followers (3.3 V or less). It represents the counterpart to Celldrain and provides the unit cell source follower current. The current is adjusted by the bias voltage V_{biasgate} . Vbiaspower can be reduced to decrease the on-chip power consumption and some of the charge-injection effects in the pixel. However, it must stay higher than the

highest detector voltage + (~1.6 V) in order to avoid non-linearities in the source follower readout. Vbiaspower should be capacitively blocked to gnda with $C \geq 100$ nF or connected to vdda.

2.2 Analog Bias Voltages

Dsub: Detector substrate voltage ($0 \text{ V} < D_{\text{sub}} < V_{\text{max}}$). The maximum voltage V_{max} for 100 kHz operation is ~1.7 V if the output source follower is disabled. It might decrease to as low as 1 V if the output source follower or the 5 MHz speed option is enabled. The actual Dsub voltage depends on the detector and the required detector bias voltage given by the difference between Dsub and Vreset. For p-on-n detectors (p-diode in n-substrate) Dsub needs to be higher than Vreset and for n-on-p detectors (n-diode in p-substrate) Dsub needs to be lower than Vreset. For most detectors, the detector bias voltage $|V_{\text{reset}} - D_{\text{sub}}|$ should be less than ~0.5 V. For noise reduction purposes, the Dsub line should have a series resistor $R \sim 1$ k Ω and capacitor to gnda with $C \geq 1000$ nF.

Vreset: Detector reset voltage ($0 \text{ V} < V_{\text{reset}} < V_{\text{max}}$). The maximum voltage V_{max} for 100 kHz operation is ~1.7 V if the output source follower is disabled. It might decrease to as low as 1 V if the output source follower or the 5 MHz speed option is enabled. The actual Vreset voltage depends on the detector and the required detector bias voltage given by the difference between Dsub and Vreset. For p-on-n detectors (p-diode in n-substrate) Dsub needs to be higher than Vreset and for n-on-p detectors (n-diode in p-substrate) Dsub needs to be lower than Vreset. For noise reduction purposes, Vreset should be capacitively blocked to gnda with $C \geq 100$ nF.

Vbiasgate: Bias voltage for the current source of the pixel source follower (~ 2.4 V). The exact voltage depends on the operation mode, the temperature, the readout speed, and the required settling accuracy. It needs to be experimentally determined for the given operating conditions. In general, a higher Vbiasgate voltage decreases the current and a lower voltage increases the current. In addition, lower operating temperatures result in a decrease in the current. If Vbiaspower is lower than 3.3 V, Vbiasgate needs to be adjusted accordingly. At room temperature, the following formula can be used to maintain a current of about 10 μA for a varying Vbiaspower voltage: $V_{\text{biasgate}} = V_{\text{biaspower}} * 1.4 - 2.22 \text{ V}$.

Vnbias: Column buffer bias for nmos current source (~ 0.85 V). It is only required for 5 MHz operation. If it is not connected externally, it will be internally pulled down to 0 V (power down column buffer). The exact voltage depends on the temperature, the readout speed and the required settling accuracy. In general, a lower Vnbias voltage as well as a lower temperature decreases the quiescent current and consequently the amplifier speed and power consumption. If Vnbias is changed, Vpbias should be changed accordingly, i.e., in the opposite direction, to maintain stability.

Vpbias: Column buffer bias for pmos current source (~ 2.35 V). It is only required for 5 MHz operation. If it is not connected externally, it will be internally pulled up to 3.3 V (power down column buffer). The exact voltage depends on the temperature, the readout speed and the required settling accuracy. In general, a higher Vpbias voltage as well as a lower temperature decreases the quiescent current and consequently the amplifier speed and power consumption. If Vpbias is changed, Vnbias should be changed accordingly, i.e., in the opposite direction, to maintain stability.

Vncasc: Column buffer bias for nmos cascode (~ 1.2 V). It is only required for 5 MHz operation. If it is not connected externally, it will be internally pulled down to 0 V. The exact voltage depends on the temperature and the applied Vnbias and Vpbias voltages. In general, a higher quiescent current as well as a lower temperature requires an increase of Vncasc. However, once Vncasc is above a certain threshold (e.g., 1.2 V at room temperature), the performance depends only slightly on the actual Vncasc voltage.

Vpcasc: Column buffer bias for pmos cascode (~ 2.0 V). It is only required for 5 MHz operation. If it is not connected externally, it will internally be pulled up to 3.3 V. The exact voltage depends on the temperature

and the applied V_{nbias} and V_{pbias} voltages. In general, a higher quiescent current as well as a lower temperature requires a decrease of V_{pcasc} . However, once V_{pcasc} is below a certain threshold (e.g., 2.0 V at room temperature), the performance depends only slightly on the actual V_{pcasc} voltage.

Vbiasoutbuf: Bias voltage for 5 MHz output buffer (~ 0.85 V). It is only required for 5 MHz operation. If it is not connected externally, it will internally be pulled down to 0 V (power down output buffer). The exact voltage depends on the temperature, the readout speed, the external load, and the required settling accuracy. In general, a lower V_{nbias} voltage as well as a lower temperature decreases the quiescent current and consequently the output buffer speed and power consumption.

RefSample: Reference voltage for the column sample & hold stage ($0 \leq \text{RefSample} \leq 2 \text{ V}$). The exact meaning of RefSample is explained in Section 5.2.2 and Figure 5-5. It is important that this voltage does not exceed a certain limit (about 2 V at room temperature) because of the increasing resistance of the sample&hold switches at higher voltages. RefSample should be capacitively blocked to gnda with $C \geq 100 \text{ nF}$.

RefColbuf: Reference voltage for the column sample & hold stage ($0.8 \text{ V} \leq \text{RefColbuf} \leq 2 \text{ V}$). The exact meaning of RefColbuf is explained in Section 5.2.2 and Figure 5-5. It is important that this voltage does not exceed a certain limit (about 2 V at room temperature) because of the increasing resistance of the sample&hold switches at higher voltages. It also needs to stay above 0.8 V due to the limited input range of the column buffer. RefColbuf should be capacitively blocked to gnda with $C \geq 100 \text{ nF}$.

2.3 Analog Outputs

The HAWAII-2RG multiplexer provides 32 output channels (OutputA/B[0-31]) plus one additional reference output (RefOutA/B) and one additional window mode output (WindowOutA/B). All output pad options described in the following section apply to the 32 regular output channels as well as to the reference and the window outputs. The letters A/B at the end of the signal name refer to two individual pads per output that can be configured according to the diagram in Figure 2-1. Basically, Pad A offers three options: 100 kHz unbuffered, 100 kHz buffered, and 5 MHz unbuffered. Pad B offers the same three options plus the additional configuration for a 5 MHz buffered readout. Both pads can be used in parallel, e.g., to obtain the buffered and unbuffered signals at the same time. The main reason, however, for the two pad options per output is given by the fact that the 5 MHz output buffer adds significant capacitance (~ 6 pF) to the output line. This capacitance is visible even if the buffer is disabled. Pad A has no connection to the fast output buffer at all and therefore offers the smallest amount of parasitic capacitance. The normal bonding configuration used at Teledyne Imaging Sensors is to bond only to the B pads to minimize the line count.

The different output options are controlled by the signals CTRL1 – CTRL7. A high signal level enables the corresponding switch. Table 2.1 shows how the individual control signals are derived from logical combinations of the bits in the internal **OutputBufReg** register (cf. Table 3.2 and the external signals FASTENPAD and BUFDISABLE. In principle, the internal register bits control the switches as long as FASTENPAD (enables the fast readout mode) and BUFDISABLE (disables the output buffer mode) are low. If FASTENPAD goes high the slow options are disabled and the fast options are enabled. It needs to be noted that only the external FASTENPAD signal but not the FASTEN bit (the equivalent internal logic bit to the FASTENPAD external signal) of the internal **MiscReg** register can overrule the **OutputBufReg** register settings. If BUFDISABLE goes high, the output buffer is disabled (slow or fast mode, depending on FASTENPAD). Since it is possible to simultaneously set more than one bit of the **OutputBufReg** register to logic 1, the user has to ensure that two different output options for the same pad type (A or B) are not enabled.

In addition to the seven control bits responsible for the different pad options, the **OutputBufReg** register contains the HIGHOHM bit. This bit controls the output impedance of the unused 28 or 31 output pads in the 4 and 1 output modes, respectively (cf. *Chapter 4: Output Modes*), in the case where the unbuffered slow readout option is selected. If HIGHOHM = 0, the unused pads are pulled up by the internal current source of the pixel source follower. If HIGHOHM = 1, these pads are brought into a high ohmic state allowing them to be connected to any desired external voltage. In all other cases, i.e., slow buffered output, fast buffered output, or fast unbuffered output, the unused pads are high ohmic irrespective of the state of the HIGHOHM bit.

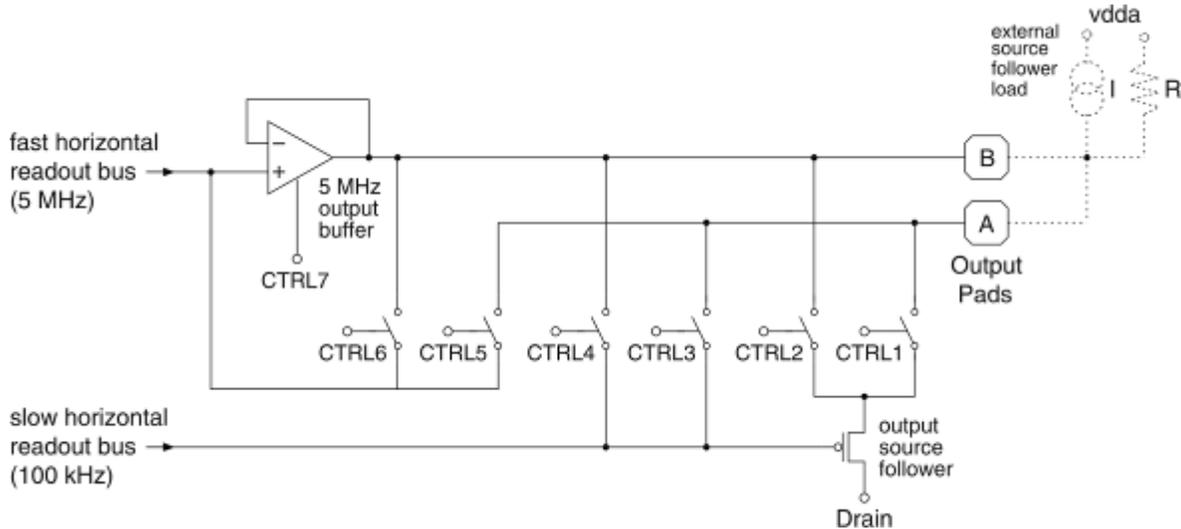


Figure 2-1: Circuit diagram illustrating the various output pad configurations

Table 2.1: Explanation of internal control signal generation

Control Signal	Logical Combination FASTENPAD and BUFDISABLE are external control signals, SFENA/B, NOSFA/B, NOFBUFA/B and FASTBUF are bits of the internal register OutputBufReg .
CTRL1	SFENA AND (NOT FASTENPAD) AND (NOT BUFDISABLE)
CTRL2	SFENB
CTRL3	NOSFA OR ((NOT FASTENPAD) AND BUFDISABLE)
CTRL4	NOSFB
CTRL5	NOFBUFA OR (FASTENPAD AND BUFDISABLE)
CTRL6	NOFBUFB
CTRL7	FASTBUF OR (FASTENPAD AND (NOT BUFDISABLE))

The slow unbuffered output mode represents the most power-saving readout mode since the pixel source follower directly drives the signal off-chip. However, this mode is insufficient to drive a large load capacitance, e.g., a long external cable, in a reasonable time. Therefore, it is particularly suited for the situation where the next signal processing stage (amplifier, ADC, sample&hold, etc.) is close and does not have a large input capacitance. The output impedance in this mode depends on both the temperature and the amplifier bias current, which is controlled by the external bias voltage Vbiasgate. Some simulation results for the output impedance of the slow unbuffered output mode are given in Table 2.2.

Table 2.2: Output Impedance for the slow unbuffered output mode

Temperature	Amplifier current	Output Impedance
300 K	5 μ A	24 k Ω
300 K	10 μ A	17 k Ω
70 K	5 μ A	10 k Ω
70 K	10 μ A	7 k Ω

For the buffered slow readout mode (100 kHz), an external current source or resistor is required as a load for the internal source follower transistor (see dotted devices on the right side in Figure 2-1). The value of the resistor or current source depends on the external capacitance, the speed requirements and the temperature. In any case, an ideal current source is preferred over a simple resistor because it results in better linearity and a gain closer to unity. Some simulation results for the output impedance of the buffered slow mode are given in Table 2.3.

Table 2.3: Output Impedance for the slow buffered output mode

Temperature	Amplifier current	Output Impedance
300 K	100 μ A	750 Ω
300 K	300 μ A	400 Ω
70 K	100 μ A	300 Ω
70 K	300 μ A	160 Ω

In the unbuffered fast output mode, the 5 MHz column buffers directly drive the output pad. Since the driving capabilities are limited to 10 – 20 pF external load, this mode can be used only if the next processing stage is nearby. The power consumption in this mode is about 2 mW per output channel plus an offset of about 15 mW due to the pixel source followers. If the output buffer is enabled, up to 100 pF load can be driven. However, the power consumption will increase by up to 2 mW per channel.

2.4 Digital Clocks and Control Signals

All digital input signals are buffered internally with a CMOS input stage. The threshold voltage that distinguishes between low and high signal level is at the center of the supply voltages, i.e., about 1.6 V for a 3.3 V supply. To guarantee proper logical operation the low signal level should be below 0.8 V and the high signal level should be above 2.5 V. For the best analog performance, together with minimum power consumption, even stronger restrictions apply to the digital input signals:

$$-0.2 \text{ V} < \text{low input signal level} < 0.3 \text{ V}$$

$$3.0 \text{ V} < \text{high input signal level} < 3.5 \text{ V}$$

On the one hand, digital input signal levels outside the recommended power supply voltage ranges can forward-bias the diodes in the pad protection circuitry leading to a high current and circuit “glow.” On the other hand, signal levels inside (between) the recommended voltage supply ranges can partly turn on the internal digital buffers and cause a significant quiescent current. Additional timing requirements for the control clocks are given in Section 5.1.1.

FSYNCB: Frame Synchronization Bar (input, active-low). FSYNCB prepares the vertical scanner for the readout of a new frame. Depending on the selected readout mode, it loads the vertical (slow) shift register with the first address bit or a specific bit pattern. Detailed explanations of its operation can be found in

Chapter 5: Readout Clocking Schemes. At the same time, the FSYNCB signal can be used in place of the DATAIN line for programming the serial interface. Please refer to *Chapter 3: Serial Interface* for further explanations.

VCLK: Vertical Shift Register Clock (input). It controls the shift register of the vertical (slow) scanner. Every falling edge of VCLK advances the pattern in the shift register by one cell (row). Detailed explanations of its operation can be found in *Chapter 5: Readout Clocking Schemes.* At the same time, the VCLK signal can be used in place of the DATACLK line for programming the serial interface. Please refer to *Chapter 3: Serial Interface* for further explanations.

VRESETB: Vertical Reset Bar (input, active-low). A low signal level resets the shift register cells of the vertical (slow) scanner. The same action can be achieved by setting the VRSTB bit of the internal MiscReg register to 0. An internal pull-up resistor keeps VRESETB high if there is no external signal driving the pin. This reset signal is only required when using the enhanced clocking mode. In normal clocking mode, the FSYNCB signal automatically performs the shift register reset when starting a new frame. Please refer to *Chapter 5: Readout Clocking Schemes,* and in particular to Section 5.3.1, for further explanations.

LSYNCB: Line Synchronization Bar (input, active-low). LSYNCB prepares the horizontal scanner for the readout of a new line. Depending on the selected readout mode, it loads the horizontal (fast) shift register with the first address bit or a specific bit pattern. Detailed explanations of its operation can be found in *Chapter 5: Readout Clocking Schemes.*

HCLK: Horizontal Shift Register Clock (input). It controls the shift register of the horizontal (fast) scanner. Every falling edge of HCLK (or every edge, if the on-chip clock divider is disabled) advances the pattern in the shift register by one cell (column). Detailed explanations of its operation can be found in *Chapter 5: Readout Clocking Schemes.*

HRESETB: Horizontal Reset Bar (input, active-low). A low signal level resets the shift register cells of the horizontal (fast) scanner. The same action can be achieved by setting the HRSTB bit of the internal MiscReg register to 0. An internal pull-up resistor keeps HRESETB high if there is no external signal driving the pin. This reset signal is only required when using the enhanced clocking mode. In normal clocking mode, the LSYNCB signal automatically performs the shift register reset when starting a new line. Please refer to *Chapter 5: Readout Clocking Schemes,* and in particular to Section 5.3.2, for further explanations.

READEN: Read Enable (input). It connects all pixels that belong to the row currently selected by the vertical scanner to the individual vertical read busses. An internal pull-up resistor keeps READEN high if there is no external signal driving the pin. Detailed explanations can be found in *Chapter 5: Readout Clocking Schemes,* particularly in Figure 5-3.

RESETEN: Reset Enable (input). It performs a reset of all pixels that are currently selected by the vertical and horizontal scanner. It also updates the flipflops that store the positions of the columns selected for reset by the horizontal scanner. Please refer to *Chapter 5: Readout Clocking Schemes* and to *Chapter 6: Reset Modes* for further explanations, particularly to Figure 5-3.

VERTWMEN: Vertical Window Mode Enable (input). It enables the window mode of the vertical (slow) scanner. Besides VERTWMEN, the VWMEN bit of the internal MiscReg register can also turn on the vertical window mode. Therefore, the window mode is disabled only if both the input signal VERTWMEN and the bit VWMEN, are 0. An internal pull-down resistor keeps VERTWMEN low if there is no external signal driving the pin. Please refer to Section 5.4 for detailed information about the window readout mode.

HORIWMEN: Horizontal Window Mode Enable (input). It enables the window mode of the horizontal (fast) scanner. Besides HORIWMEN, the HWMEN bit of the internal **MiscReg** register can also turn on the horizontal window mode. Therefore, the window mode is disabled only if both the input signal HORIWMEN and the bit HWMEN, are 0. An internal pull-down resistor keeps HORIWMEN low if there is no external signal driving the pin. Please refer to Section 5.4 for detailed information about the window readout mode.

VREADEDGE: Vertical Reading Edge (input). This signal is only required for the enhanced clocking mode of the vertical scanner. It selects which edge of the bit pattern in the vertical shift register defines the location of the line currently selected for read. A logical 0 selects the rising edge, a logical 1 selects the falling edge. The same selection can be done with the VEDGE bit of the internal **NormalModeReg** register (full field readout mode) or with the VEDGWM bit of the internal **WindowModeReg** register (window readout mode). The internal bits and the external VREADEDGE signal are logically combined by an OR-gate allowing operation to switch to the falling edge with either a high internal bit or a high VREADEDGE signal. The rising edge is selected only if both the internal bit and VREADEDGE signal are low. An internal pull-down resistor keeps VREADEDGE low if there is no external signal driving the pin. Please refer to Section 5.3.1 for further information on the enhanced clocking mode.

HREADEDGE: Horizontal Reading Edge (input). This signal is only required for the enhanced clocking mode of the horizontal scanner. It selects which edge of the bit pattern in the horizontal shift register defines the location of the line currently selected for read. A logical 0 selects the rising edge, a logical 1 selects the falling edge. The same selection can be done with the HEDGE bit of the internal **NormalModeReg** register (full field readout mode) or with the HEDGWM bit of the internal **WindowModeReg** register (window readout mode). The internal bits and the external HREADEDGE signal are logically combined by an OR-gate allowing operation to switch to the falling edge with either a high internal bit or a high HREADEDGE signal. The rising edge is selected only if both the internal bit and HREADEDGE signal are low. An internal pull-down resistor keeps HREADEDGE low if there is no external signal driving the pin. Please refer to Section 5.3.2 for further information on the enhanced clocking mode.

SAMPLECLK: Sample Clock (input). It switches between the two capacitor banks of the column buffer sample&hold stages. The same switching can be done with the SAMPCLK bit of the internal **MiscReg** register. The internal SAMPCLK bit and the external SAMPLECLK signal are logically combined by an OR-gate. Therefore, if one of the two signals is not being used, it should stay low to allow the other signal to control the sample&hold stages. An internal pull-down resistor keeps SAMPLECLK low if there is no external signal driving the pin. The SAMPLECLK signal is required only in the fast readout mode (5 MHz). Please refer to Section 5.2.2 for further information on the fast readout mode.

CSB: Chip Select Bar (input, active-low). It selects the multiplexer for the serial programming interface by the serial control lines DATACLK and DATAIN (or VCLK and FSYNCB if line sharing is activated). An internal pull-up resistor keeps CSB high if there is no external signal driving the pin. Detailed explanations about the CSB signal can be found in *Chapter 3: Serial Interface*.

DATACLK: Data Clock (input). It is the clock signal for the serial programming interface. If line sharing is enabled, i.e., VCLK is used as the serial clock, DATACLK has to stay low in order not to interfere with the VCLK signal. An internal pull-down resistor keeps DATACLK low if there is no external signal driving the pin. Additional information about the DATACLK signal can be found in *Chapter 3: Serial Interface*.

DATAIN: Data Input (input). It is the data input signal for the serial programming interface. If line sharing is enabled, i.e., FSYNCB is used as the serial data line, DATAIN has to stay high in order not to interfere with the FSYNCB signal. An internal pull-up resistor keeps DATAIN high if there is no external signal driving the pin. Additional information about the DATAIN signal can be found in *Chapter 3: Serial Interface*.

DATAOUT: Data Output (output). It is the data output signal for the serial programming interface. The DATAOUT line “echoes” the DATAIN input bits at the output of the last cell of the serial shift register. It can also be used to program several multiplexers with the same set of lines. Please refer to *Chapter 3: Serial Interface* for further information on the DATAOUT signal.

MAINRESETB: Main Reset Bar (input, active-low). A low MAINRESETB signal resets the shift register of the serial interface and sets the internal mode selection registers to the default values (cf. Table 3.2). An internal pull-up resistor keeps MAINRESETB high if there is no external signal driving the pin. Please refer to *Chapter 3: Serial Interface* for further explanations on the MAINRESETB signal.

VTESTEN: Vertical Test Output Enable (input). It enables the output signal FRAMECHK, which indicates the end of a readout frame, i.e., the last cell of the vertical shift register has been reached. FRAMECHK can also be enabled by the VTESTEN bit of the internal **GainReg** register. If FRAMECHK needs to be disabled, both the VTESTEN signal and the VTESTEN bit have to be low. An internal pull-down resistor keeps VTESTEN low if there is no external signal driving the pin. For further information, see *Chapter 5: Readout Clocking Schemes*.

HTESTEN: Horizontal Test Output Enable (input). It enables the output signal LINECHK, which indicates the end of a readout line, i.e. the last cell of the horizontal shift register has been reached. LINECHK can also be enabled by the HTESTEN bit of the internal **GainReg** register. If LINECHK needs to be disabled, both the HTESTEN signal and the HTESTEN bit have to be low. An internal pull-down resistor keeps HTESTEN low if there is no external signal driving the pin. For further information, see *Chapter 5: Readout Clocking Schemes*.

FRAMECHK: Frame Check (output). It indicates the end of a readout frame, i.e., the last cell of the vertical shift register has been reached. To use the FRAMECHK signal, it needs to be enabled either by the VTESTEN signal or by the VTESTEN bit of the internal **GainReg** register. For further information, see *Chapter 5: Readout Clocking Schemes*.

LINECHK: Line Check (output). It indicates the end of a readout line, i.e. the last cell of the horizontal shift register has been reached. To use the LINECHK signal, it needs to be enabled either by the HTESTEN signal or by the HTESTEN bit of the internal **GainReg** register. For further information, see *Chapter 5: Readout Clocking Schemes*.

MODECTRL1: Output Mode Control 1 (input). It controls, together with MODECTRL2, what output mode will be used for readout (1, 4 or 32 outputs). If MODECTRL1 and MODECTRL2 are 0, the output mode is determined by the bits MODE1, MODE2 and MODE32 of the internal **GainReg** register. Otherwise, the MODECTRL lines have priority. Please refer to *Chapter 4: Output Modes* for a detailed explanation of the MODECTRL signals.

MODECTRL2: Output Mode Control 2 (input). It controls, together with MODECTRL1, what output mode will be used for readout (1, 4 or 32 outputs). If MODECTRL1 and MODECTRL2 are 0, the output mode is determined by the bits MODE1, MODE2 and MODE32 of the internal **GainReg** register. Otherwise, the MODECTRL lines have priority. Please refer to *Chapter 4: Output Modes* for a detailed explanation of the MODECTRL signals.

BUFDISABLE: Output Buffer Disable (input). It disables the output buffer corresponding to the readout speed selected by the signal FASTENPAD. The BUFDISABLE signal also impacts the output mode through its logical combination with FASTENPAD and the output mode control lines CTRL1-7. It is important that the user ensures that the signal is logically consistent with the settings of the internal **OutputBufReg** register. Please refer to Section 2.3 for additional information about the BUFDISABLE signal.

FASTENPAD: Fast Mode Enable Pad (input). It enables the fast readout mode (5 MHz) and the corresponding buffer options for the output pads. The FASTENPAD signal also impacts the output mode through its logical combination with BUFDISABLE and the output mode control lines CTRL1-7. It is important that the user ensures that the signal is logically consistent with the settings of the internal **OutputBufReg** register. The fast mode can also be enabled by the bit FASTEN of the internal **MiscReg** register, but the output buffer options are not affected by this bit. Further explanations about the output pad options can be found in Section 2.3. For more information about the fast readout mode, see Section 5.2.2.

HCLK1: Horizontal Clock 1 (input/output). It is one of the (optional) internal non-overlapping clocks for the horizontal shift register in full field operation. The pad can be used to either monitor the internal signal (diagnostic, output) or to externally control it (less on-chip power consumption, input). In the latter case, the internal clock buffers need to be disabled by setting the PDCK bit of the internal **OptionsReg** register to 1. The relation between the HCLK input signal and the HCLK1 signal is shown in Figure 2-2. The normal bonding configuration used at Teledyne Imaging Sensors does not bond out the HCLK1 pad.

HCLK1B: Horizontal Clock 1 Bar (input/output). It is the inverted signal of HCLK1, one of the (optional) internal non-overlapping clocks for the horizontal shift register in full field operation. The pad can be used to either monitor the internal signal (diagnostic, output) or to externally control it (less on-chip power consumption, input). In the latter case, the internal clock buffers need to be disabled by setting the PDCK bit of the internal **OptionsReg** register to 1. The relation between the HCLK input signal and the HCLK1B signal is shown in Figure 2-2. The normal bonding configuration used at Teledyne Imaging Sensors does not bond out the HCLK1B pad.

HCLK2: Horizontal Clock 2 (input/output). It is one of the (optional) internal non-overlapping clocks for the horizontal shift register in full field operation. The pad can be used to either monitor the internal signal (diagnostic, output) or to externally control it (less on-chip power consumption, input). In the latter case, the internal clock buffers need to be disabled by setting the PDCK bit of the internal **OptionsReg** register to 1. The relation between the HCLK input signal and the HCLK2 signal is shown in Figure 2-2. The normal bonding configuration used at Teledyne Imaging Sensors does not bond out the HCLK2 pad.

HCLK2B: Horizontal Clock 2 Bar (input/output). It is the inverted signal of HCLK2, one of the (optional) internal non-overlapping clocks for the horizontal shift register in full field operation. The pad can be used to either monitor the internal signal (diagnostic, output) or to externally control it (less on-chip power consumption, input). In the latter case, the internal clock buffers need to be disabled by setting the PDCK bit of the internal **OptionsReg** register to 1. The relation between the HCLK input signal and the HCLK2B signal is shown in Figure 2-2. The normal bonding configuration used at Teledyne Imaging Sensors does not bond out the HCLK2B pad.

HCLKWM1, HCLKWM1B, HCLKWM2, HCLKWM2B: These (optional) clocks represent the same signals for the window readout mode as the clock HCLK1, HCLK1B, HCLK2, HCLK2B for the full field readout mode. If these pads are used to control these clock signals, the internal clock buffers need to be disabled by setting the PDCKWM bit of the internal **OptionsReg** register to 1. The relation between the HCLK input signal and the internal window mode clock signal is shown in Figure 2-2. The normal bonding configuration used at Teledyne Imaging Sensors does not bond out any of the HCLKWM or HCLKWMB pads.

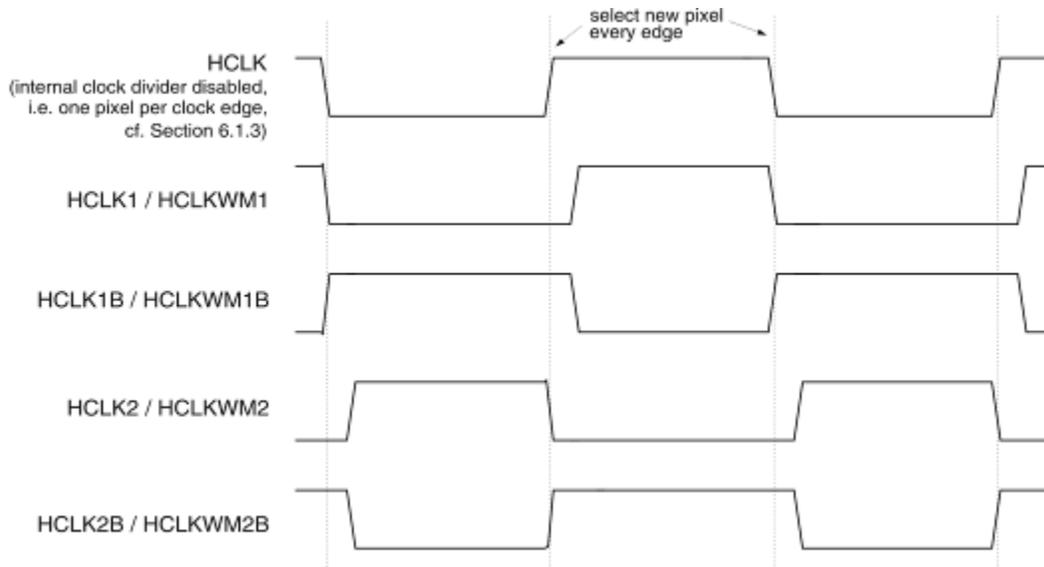


Figure 2-2: Timing diagram of the internal shift register clocks for the horizontal scanner

2.5 Temperature Sensors

The HAWAII-2RG multiplexer contains two independent temperature sensors. One sensor (Sensor 1) is located along the top edge of the multiplexer between the horizontal scanner and the pads, the other one (Sensor 2) along the other three edges of the array. Each is comprised of a long aluminum line with a resistance of approx. 40 k Ω at room temperature. Individual pads called **Temp1** for Sensor 1 and **Temp2** for Sensor 2 are connected to the two ends of each metal line. They allow the user to externally measure the resistance and, by this means, determine the FPA temperature.

In the temperature range from 300 K to 70 K, the resistance changes linearly with temperature at a rate of about $\sim 70 \Omega / K$. Below 70 K, the resistance-temperature dependence starts to flatten out. By 30 K, the rate drops to about $10 \Omega / K$. However, since the absolute resistance has also significantly dropped compared to the 40 k Ω value at room temperature, the relative resistance change per K is still comparable to the relative resistance change at room temperature. Therefore, the sensors are usable even below 30 K. It needs to be noted that due to process variations every sensor will behave slightly different and needs to be calibrated individually.

When measuring the line resistance, it has to be ensured that the current through the temperature sensors never exceeds 1 mA. In most cases, a much lower current should be used to not modify the temperature value due to the power consumption of the sensor itself. For instance, a sensor current of 1 mA would lead to a power consumption of $P = R * I^2 = 40 \text{ k}\Omega * (1 \text{ mA})^2 = 40 \text{ mW}$ at room temperature! Although the power consumption drops for lower temperatures due to the reduced resistance, it will still be on the order of mWs. Consequently, the current needs to be carefully watched during temperature measurements. On the other hand, a small current limits the temperature resolution because it leads to a smaller voltage drop across the resistor. Depending on the requirements for the application (operating temperature, required temperature resolution), an appropriate tradeoff for the sensor current needs to be found.

3 Serial Interface

The 3-wire serial interface allows programming of the internal registers of the HAWAII-2RG multiplexer. These registers are used to set the desired operation mode and to control the window position for the window readout mode.

The three required lines are CSB (ChipSelectBar), DATACLK and DATAIN. In order to save lines, the DATACLK and DATAIN lines can be shared with the VCLK and FSYNCB signals for the vertical scanner. In this case, the level of CSB decides whether the vertical scanner (CSB high) or the serial interface logic (CSB low) listens to the DATACLK/VCLK and DATAIN/FSYNCB signals. The line sharing can be disabled or enabled using the IFCTRL bit of the internal **OptionsReg** register (Table 3.2). It must be disabled if the interface and the vertical scanner need to be clocked at the same time.

Each programming cycle consists of 16 bits that are clocked into the multiplexer on the rising edge of DATACLK. The MSB (bit 15) has to be sent first, the LSB (bit 0) last. CSB has to go low before and go high after the programming cycle (the serial interface is enabled only while CSB is low). The 16 bits are divided into 4 address and 12 data bits. The rising edge of CSB decodes the address bits and transfers the data into the corresponding registers. The exact timing diagram is shown in Figure 3-1.

Timing:

Table 3.1 contains the minimum timing requirements for the different intervals t1 – t8. There is no maximum timing restriction.

Important: The rise and fall time requirements for the control signals CSB, DATACLK and DATAIN are very relaxed (< 200 ns or even longer for low noise signals). However, at least half the rise/fall time should be added to the parameters t1 – t8 if the rise/fall times are > 10 ns.

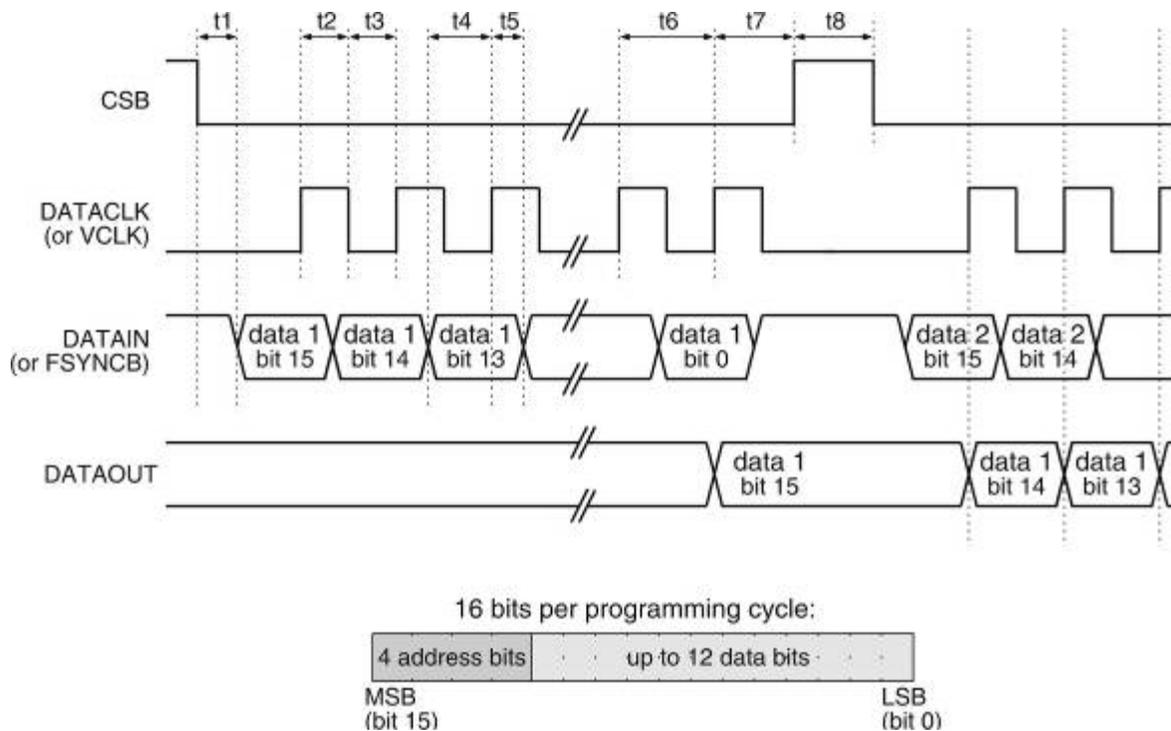


Figure 3-1: Timing diagram for the serial programming interface

Table 3.1: Timing intervals for the serial interface

Timing parameter	Minimum time	Description
t1	15 ns	CSB falling edge to first data bit, only required if FSYNCB is used (to avoid resetting of the slow scanner)
t2	15 ns	Positive DATACLK pulse width
t3	10 ns	Negative DATACLK pulse width
t4	10 ns	DATAIN settling time
t5	10 ns	DATAIN hold time
t6	25 ns	Full DATACLK cycle width
t7	25 ns	Last DATACLK rising edge to CSB rising edge
t8	50 ns	Internal data decoding and interpretation time

DATAOUT:

In addition to the 3 interface control lines, there is one line (DATAOUT) that outputs the programmed bit pattern with a delay of 16 clock cycles. It can be used to connect several multiplexers in a daisy-chain configuration: The DATAOUT signal of the first mux is connected to the DATAIN pin of the second mux, DATAOUT of the second mux is connected to DATAIN of the third mux and so on. Using this configuration, all muxes can be programmed with the same 3 lines (DATACLK and CSB are shared by all muxes, DATAIN goes only into the first mux). The total number of bits to be transmitted is now 16 bits times the number of muxes in the chain. The 16 bits for the last mux have to be sent first, the ones for the first mux need to be sent last.

Important: In order to use the DATAOUT pin, it first has to be enabled by setting the DOEN bit in the internal register **OptionsReg** (cf. Table 3.2). By default, the DATAOUT pin is disabled because its strong output buffer could be a potential noise and glow source.

MAINRESETB:

The MAINRESETB signal allows the user to set all internal registers back to their default values (see Table 3.2). It needs to be pulled low for about 100 ns in order to perform this task. If not connected, it will be pulled up internally by a 10 MΩ resistor. The reset cycle should be applied after every power-up, otherwise the register values are not defined. In applications without a need for the serial interface, the MAINRESETB line can be pulled down permanently. This ensures that the register values cannot be changed accidentally.

Internal Registers:

The internal mode and window address registers consist of single event upset (SEU) proof flip-flops. This ensures that the multiplexer does not accidentally change its mode of operation due to radiation effects. Table 3.2 explains the internal register space. The HAWAII-2RG multiplexer has 13 internal registers with varying bit widths from 4 to 11 bits. The first column gives the register name, the second column the register address (bits 15 – 12 of the 16 bit serial word). The third column shows the bit width of the register. The next two columns contain the individual register bit numbers, the bit names and the default value. The bit numbers in the register corresponds to the bit numbers of the transmitted 16 bit serial word (e.g. bit 0 = bit 0, bit 1 = bit 1, etc.). Finally, a short description is given for each individual control bit in the last column.

Table 3.2: Internal Register Description

Register Name	Address (binary)	Reg. Width	Bit #	Bit Name	Default Settings	Description
NOP	0000	0			x	No Operation
HoriDirReg (see Chapter 4: Output Modes)	0001	8				Scanning directions of the horizontal scanner: 0 = left to right, 1 = right to left
			0	HINVDIR0	0	32 output mode: 64-column subblocks # 0,2,4,6 of the left 512-column block 4 output mode: left 512-column block 1 output mode: complete array
			1	HINVDIR1	1	32 output mode: 64-column subblocks # 1,3,5,7 of the left 512-column block 4 & 1 output mode: no meaning
			2	HINVDIR2	0	32 output mode: 64-column subblocks # 8,10,12,14 of the next 512-column block 4 & 1 output mode: no meaning
			3	HINVDIR3	1	32 output mode: 64-column subblocks # 9,11,13,15 of the next 512-column block 4 output mode: next 512-column block 1 output mode: no meaning
			4	HINVDIR4	0	32 output mode: 64-column subblocks # 16,18,20,22 of the next 512-column block 4 output mode: next 512-column block 1 output mode: no meaning
			5	HINVDIR5	1	32 output mode: 64-column subblocks # 17,19,21,23 of the next 512-column block 4 & 1 output mode: no meaning
			6	HINVDIR6	0	32 output mode: 64-column subblocks # 24,26,28,30 of the right 512-column block 4 & 1 output mode: no meaning
			7	HINVDIR7	1	32 output mode: 64-column subblocks # 25,27,29,31 of the right 512-column block 4 output mode: right 512-column block 1 output mode: no meaning
GainReg	0010	8	3 - 0	GAIN	0	Column buffer gain for the fast (5 MHz) readout mode, gain = data + 1
			4	CAPEN	1	Enable compensation cap to suppress column buffer oscillations at low gain
			5		x	Unused
			6	VTESTEN	0	Enable test output of vertical scanner
			7	HTESTEN	0	Enable test output of horizontal scanner <i>note: test outputs can also be enabled by the input signals VTESTEN and HTESTEN</i>
OutputModeReg	0011	8	0	MODE1	0	Enable 1 output mode
			1	MODE4	1	Enable 4 output mode

Register Name	Address (binary)	Reg. Width	Bit #	Bit Name	Default Settings	Description
			2	MODE32	0	Enable 32 output mode <i>note: The input signals MODECTRL1 and MODECTRL2 have higher priority than the bits MODE1, MODE4 and MODE32</i>
			3	WMOUTEN	0	1 = Use separate window output 0 = Use output #7 as window output
			4	REFPIXEN	1	Enable separate reference output derived from a single reference pixel
			5	REFMODE	1	Reference output mode: 1 = ref. pixel is permanently connected to the ref. voltage (Dsub or Vreset) 0 = ref. pixel is connected to the ref. voltage (Dsub or Vreset) only during the reset phase of the upper left array pixel
			6	REFVOLT	1	Selects the reference voltage for the pixel of the separate reference output: 1 = Dsub, 0 = Vreset
			7	REFROW	0	Enables the extra row of reference pixels on top of the normal pixel array
OutputBufReg (see Section 2.3)	0100	8	0	SFENA	1	Enable source follower buffer for output pad A in slow readout mode (100 kHz)
			1	SFENB	0	Enable source follower buffer for output pad B in slow readout mode (100 kHz)
			2	NOSFA	0	Enable direct (unbuffered) output for pad A in slow readout mode (100 kHz)
			3	NOSFB	0	Enable direct (unbuffered) output for pad B in slow readout mode (100 kHz)
			4	HIGHOHM	1	Put outputs not being used into a high ohmic state (only for unbuffered output)
			5	FASTBUF	0	Enable output buffer for output pad B in fast readout mode (5 MHz)
			6	NOFBUFA	0	Enable direct (unbuffered) output for pad A in fast readout mode (5 MHz)
			7	NOFBUFFB	0	Enable direct (unbuffered) output for pad B in fast readout mode (5 MHz) <i>note: The input signals BUFFERDISABLE and FASTENPAD also affect the buffer settings and may have priority over OutputBufReg</i>
NormalModeReg	0101	8				Normal (full field) scanning mode only
			0	VMODE	0	0 = standard clocking (vertical scanner) 1 = enhanced clocking (vertical scanner)
			1	HMODE	0	0 = standard clocking (horiz. scanner) 1 = enhanced clocking (horiz. scanner)
			2	VINVDIR	0	Scanning direction for vertical scanner: 0 = top to bottom, 1 = bottom to top
			3		x	unused

Register Name	Address (binary)	Reg. Width	Bit #	Bit Name	Default Settings	Description
			4	VEDGE	0	Select active edge of the bit pattern in the vertical shift register for reading (enhanced clocking): 0=rising, 1=falling
			5	HEDGE	0	Select active edge of the bit pattern in the horizontal shift register for reading (enhanced clocking): 0=rising, 1=falling <i>note: bit 4 & 5 can be overruled by the input signals VREADEDGE and HREADEDGE</i>
			6	RSTEDGE	0	Select active edge of the bit pattern in the vertical shift register for reset (enhanced clocking): 0=rising, 1=falling
			7	GLOBAL	0	Enable global reset
WindowModeReg (first part)	0110	8				Window scanning mode only
			0	VMODWM	0	0 = standard clocking (vertical scanner) 1 = enhanced clocking (vertical scanner)
			1	HMODWM	0	0 = standard clocking (horiz. scanner) 1 = enhanced clocking (horiz. scanner)
			2	VDIRWM	0	Scanning direction for vertical scanner: 0 = top to bottom, 1 = bottom to top
			3	HDIRWM	0	Scanning direction for horiz. scanner: 0 = left to right, 1 = right to left
			4	VEDGWM	0	Select active edge of the bit pattern in the vertical shift register for reading (enhanced clocking): 0=rising, 1=falling
WindowModeReg (second part)	0110	8	5	HEDGWM	0	Select active edge of the bit pattern in the horizontal shift register for reading (enhanced clocking): 0=rising, 1=falling <i>note: bit 4 & 5 can be overruled by the input signals VREADEDGE and HREADEDGE</i>
			6	REDGWM	0	Select active edge of the bit pattern in the vertical shift register for reset (enhanced clocking): 0=rising, 1=falling
			7	GLOBWM	0	Enable global reset (inside the window)
MiscReg	0111	7	0	VWMEN	0	Enable window mode for vertic. scanner
			1	HWMEN	0	Enable window mode for horiz. scanner <i>note: bits 0 and 1 can be overruled by the input signals VERTWMEN and HORIWMEN</i>
			2	VRSTB	1	Setting this bit to 0 resets the shift register of the vertical scanner
			3	HRSTB	1	Setting this bit to 0 resets the shift register of the horizontal scanner <i>note: bits 2 and 3 can be overruled by the input signals VRESETB and HRESETB</i>
			4	FASTEN	0	Enables the fast readout mode (5 MHz) <i>note: can be overruled by FASTENPAD sig.</i>

Register Name	Address (binary)	Reg. Width	Bit #	Bit Name	Default Settings	Description
			5	SAMPCLK	0	Controls the sample&hold stages in the column buffers <i>note: can be overruled by SAMPLECLK sig.</i>
			6	CLKMOD	0	0 = one pixel per HCLK cycle (required for fast readout operation) 1 = one pixel per HCLK edge
VertStartReg	1000	11	10 - 0	VSTART	0	Vertical start address of sub-window
VertStopReg	1001	11	10 - 0	VSTOP	2047	Vertical stop address of sub-window
HoriStartReg	1010	11	10 - 0	HSTART	0	Horizontal start address of sub-window
HoriStopReg	1011	11	10 - 0	HSTOP	2047	Horizontal stop address of sub-window
PowerDownReg (see Chapter 8: Power Down Control)	1100	8	0	PDREF0	1	Power down ref. output on the rising edge of LINECHK (Full field Mode)
			1	PDREF1	0	Power down ref. output when resetting the horizontal shift reg. (Full field Mode)
			2	PDREF2	1	Power down ref. output on the rising edge of LINECHK (Window Mode)
			3	PDREF3	0	Power down ref. output when resetting the horiz. scanner shift reg (Window Mode)
			4	PDBUF0	1	Power down fast output buffers on the rising edge of LINECHK (Full field Mode)
			5	PDBUF1	0	Power down fast output bufs when resetting the horiz. shift reg (Full field Mode)
			6	PDBUF2	1	Power down fast output buffers on the rising edge of LINECHK (Window Mode)
			7	PDBUF3	0	Power down fast output bufs when resetting the horiz. shift reg (Window Mode)
OptionsReg	1101	4	0	PDCK	0	Power down internal clock buffers for horizontal scanner (normal mode)
			1	PDCKWM	0	Power down internal clock buffers for horizontal scanner (window mode)
			2	IFCTRL	0	1 = VCLK and FRAMESYNC do not affect the serial interface 0 = VCLK and FRAMESYNC can be used to control the serial interface (DATACLK and DATAIN not needed)
			3	DOEN	0	Enable the DATAOUT signal of the serial interface

4 Output Modes

The HAWAII-2RG multiplexer offers three different output modes that allow the user to read the pixel data through either 1, 4 or 32 output channels. The single output option has the lowest power consumption but also the longest readout time. The 32 output option offers the maximum frame rate at a cost of higher power consumption and greater external electronics effort. The 4 output mode represents a tradeoff that delivers moderate frame speed combined with low power consumption and a small number of external output channels. All three options can be operated at the slow (100 kHz) or the fast (5 MHz) readout speed. Table 4.1 shows a comparison between the individual frame times for 1, 4 and 32 output channels and the two possible pixel rates.

Table 4.1: Frame times for the different output modes

Output Mode	Pixel Rate	Frame Time (2048 x 2048 pixels)
1 output	100 kHz	42 s
	5 MHz	840 ms
4 outputs	100 kHz	10.6 s
	5 MHz	210 ms
32 outputs	100 kHz	1.36 s
	5 MHz	28 ms

The output mode selection is controlled by the external signals MODECTRL1 and MODECTRL2 as well as the internal bits MODE1, MODE4 and MODE32 in the internal **OutputModeReg**. Table 4.2 explains the correlation between the control signal levels and the corresponding output modes. Basically, as soon as either MODECTRL1 or MODECTRL2 is high, the register settings in **OutputModeReg** will be overruled by the external settings of the MODECTRL1/2 signals. When using the internal register settings, it needs to be ensured that only one of the three MODE1/4/32 bits is set to one at a given time.

Table 4.2: Explanation of the output mode selection

MODECTRL1	MODECTRL2	Output Mode
0	0	Determined by the internal bits MODE1, MODE4 and MODE32 of the OutputModeReg (see Table 3.2)
1	0	1 output
0	1	4 outputs
1	1	32 outputs

The individual array sub-blocks assigned to the different output channels are rectangular with a height of 2048 pixels and a width of (2048 / number of outputs) pixels. This means that the number of pixels per row, which corresponds to the number of clock cycles for the horizontal scanner, depends on the selected output mode. The relevant timing diagrams in *Chapter 5: Readout Clocking Schemes* and *Chapter 6: Reset Modes* therefore always contain three different numbers of HCLK cycles corresponding to the three possible output modes. It needs to be noted that the window readout mode, in contrast to the full field mode (cf. Section 5.4), is read through one single output, regardless of the selected output mode. The following sections explain the three full field output mode options in more detail.

4.1 1-Output Mode

In the single output mode, all 2048 x 2048 pixels are read through Output #7. The horizontal scanning direction is controlled by the HINVDIR0 bit of the internal **HoriDirReg** register (cf. Table 3.2). The VINVDIR bit of the internal **NormalModeReg** controls the vertical scanning direction in full field mode. Figure 4-1 illustrates the scanning directions for the single output mode.

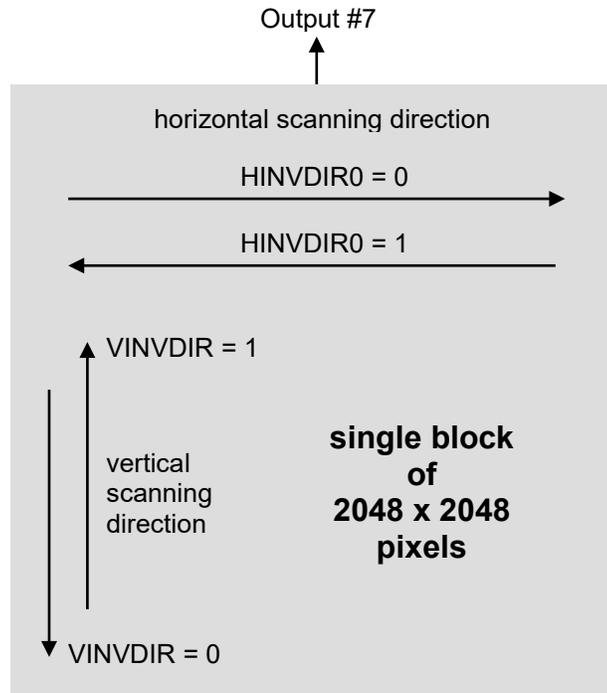


Figure 4-1: Illustration of the single output mode

4.2 4-Output Mode

The 4-output mode represents the default mode which will be automatically activated after a reset of the internal mode registers (cf. external MAINRESETB signal in Section 2.4). The left 512 x 2048 block is read through Output #7, the next block through Output #15, the next block through Output #23, and the right block through Output #31. The horizontal scanning direction of the left block is controlled by the HINVDIR0 bit, the next block by the HINVDIR3, the next block by the HINVDIR4, and the right block by the HINVDIR7 bit of the internal **HoriDirReg** register. The VINVDIR bit of the internal **NormalModeReg** controls the vertical scanning direction of all four sub-blocks. Figure 4-2 illustrates the pixel arrangement and the scanning directions for the 4-output mode.

4.3 32-Output Mode

In the 32-output mode, the array is divided into 32 sub-blocks of 64 x 2048 pixels each. Every sub-block is read through a separate output channel, starting with Output #0 on the far left side and ending with Output #31 on the far right side. The horizontal scanning directions are controlled by the bits HINVDIR0 to HINVDIR7 of the internal **HoriDirReg** register according to the illustration in Figure 4-3. Like in the previous output modes, a logical 0 means scanning from left to right and a logical 1 means scanning from right to left. The VINVDIR bit of the internal **NormalModeReg** controls the vertical scanning direction of all 32 sub-blocks.

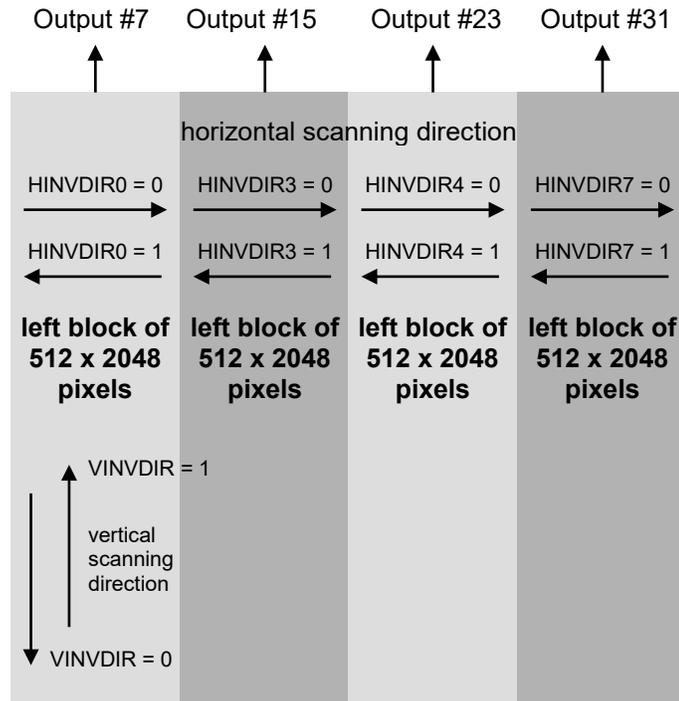


Figure 4-2: Illustration of the 4-output mode

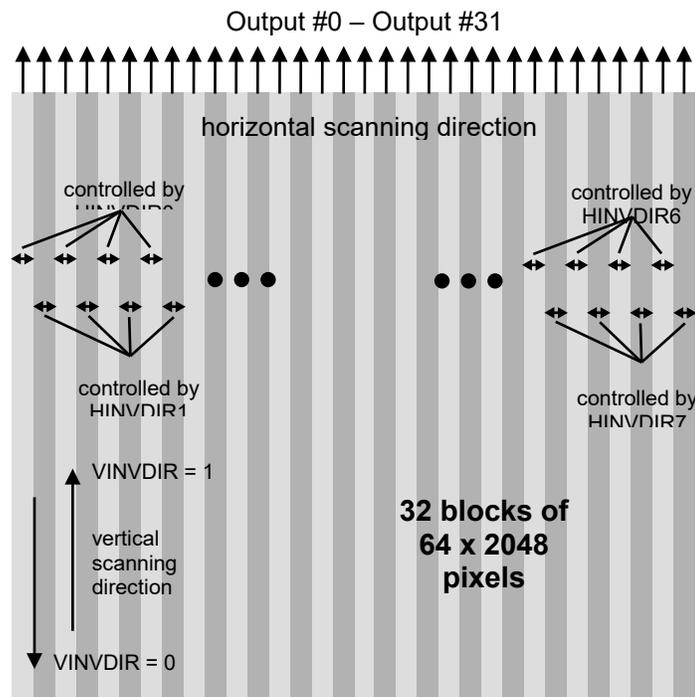


Figure 4-3: Illustration of the 32-output mode

5 Readout Clocking Schemes

This chapter describes the different clock patterns that can be used to read out the HAWAII-2RG multiplexer. Depending on the requirements, an appropriate scheme can be chosen. The slow readout mode allows lowest power operation together with low read noise while the fast readout mode gives higher frame rates at the cost of higher power and increased read noise. Optimized readout for integration times shorter than a frame time or even a row time can be achieved with the enhanced clocking mode. It is also possible to switch at any time between the various readout schemes. For example, it is possible to read out the full field in slow mode and the selected sub-window in fast mode. In addition, the window guide mode enables a parallel operation of full field and window mode using an interleaved clocking and readout pattern. That means a long integration time for the full field and a short integration time for the sub-window can be implemented simultaneously.

5.1 General Clocking Requirements

5.1.1 Signal level and timing

All digital control signals need to have 3.3 V CMOS levels, i.e. 0 V for a low and 3.3 V for a high signal level. It is important that the overshoot during a level change does not exceed 200 mV in order to prevent the ESD protection diodes from getting forward biased. A higher overshoot can lead to a significant parasitic current in the protection diodes and, as a consequence, to a considerable emission of photons (glow). At the same time, the digital high signal levels should not be less than $V_{DD} - 300 \text{ mV} = 3.0 \text{ V}$ or the digital low signal levels more than $GND + 300 \text{ mV} = 300 \text{ mV}$. Otherwise, the internal clock buffers start showing a large quiescent current resulting in another possible glow source. These requirements are summarized in Table 5.1. Further detailed explanation of the individual signals can be found in Section 2.4.

The clock rise and fall time requirements, in general, are not very stringent since all clocks are internally buffered. For the slow mode, rise times of 100 ns or even more can be used. However, the longer the rise time, the higher the uncertainty of the actual switching point and the lower the noise immunity. For the HAWAII-2RG design, Schmidt triggers are added to the inputs to all of the clocks at the bond pads. This technique, common to modern CMOS design, greatly hardens the multiplexer against spurious clocking due to noise or reflections in long cables. Therefore, Table 5.1 shows some general guide lines for the rise and fall times which should be used for best performance.

Table 5.1: General requirements for digital control and clock signals

Property	Requirements for Slow Operation (100 kHz)	Requirements for Fast Operation (5 MHz)
Rise time	< 80 ns	< 30 ns
Fall time	< 80 ns	< 30 ns
Separation of two consecutive signal edges	> 100 ns (T > 150 K) > 80 ns (T < 150 K)	> 70 ns (T > 150 K) > 50 ns (T < 150 K)
Low signal level	-0.2 V to 0.3 V	-0.2 V to 0.3 V
High signal level	3.0 V to 3.5 V	3.0 V to 3.5 V

The table entry “separation of two consecutive signal edges” refers to consecutive edges of the same signal (e.g., rising edge followed by falling edge) as well as to consecutive edges of different signals if they are drawn as non-overlapping edges in the corresponding timing diagram. This separation time is required for the internal evaluation of the applied signal change. Because the internal buffers become faster with lower temperature, the minimum separation time becomes shorter for lower temperatures. The separation time is measured from the middle of the first edge to the middle of the second edge and is independent of the rise and fall times. Since Table 5.1 only takes into account the digital scanner logic, additional restrictions might apply to certain clock signals due to the analog multiplexer performance. As an example, the maximum

frequency for HCLK in slow readout mode is 100 kHz due to the required settling time (assuming 11τ settling driving 300pF of capacitance; under less stringent conditions the slow mode has been successfully operated at 500 kHz frequency). The timing requirements described in Table 5.1 apply to all timing diagrams in this manual and are not mentioned again at the individual timing discussions.

5.1.2 Analog sampling for external A/D conversion

If the analog multiplexer output is externally sampled and converted into a digital signal, the actual sampling point is important for optimal performance. Most A/D converters require a sampling or conversion pulse that initiates the internal conversion cycle. For maximum settling time, this pulse should occur right before switching to a new pixel. However, the rising edge of the conversion pulse (or falling edge for active-low conversion pulses) must not overlap the falling edge of HCLK, which triggers the selection of a new pixel. Otherwise, a distortion of the current pixel value might occur. The corresponding timing diagram is shown in Figure 5-1. The separation time Δt_{sample} between the conversion pulse edge and the HCLK edge depends on the rise and fall times t_{rise} as well as on the internal ADC delay time t_{delay} between conversion pulse and actual sampling point. The absolute minimum separation time is $\Delta t_{\text{sample}} = t_{\text{rise}} + t_{\text{delay}}$, but should be somewhat increased to provide an additional safety margin. The position of the falling edge of the conversion pulse (or rising edge for active low signal) is determined by the ADC constraints for pulse width and cycle time.

Note: Under certain conditions, the conversion pulse might come closer to the falling HCLK edge since the multiplexer shows an internal delay between the HCLK edge and the change in the analog output signal. In this case, however, the performance significantly depends on the design of the external system. Any crosstalk between clock lines and analog signal lines can degrade the system performance. It is therefore not recommended to decrease Δt_{sample} below the limit given above unless required for other reasons.

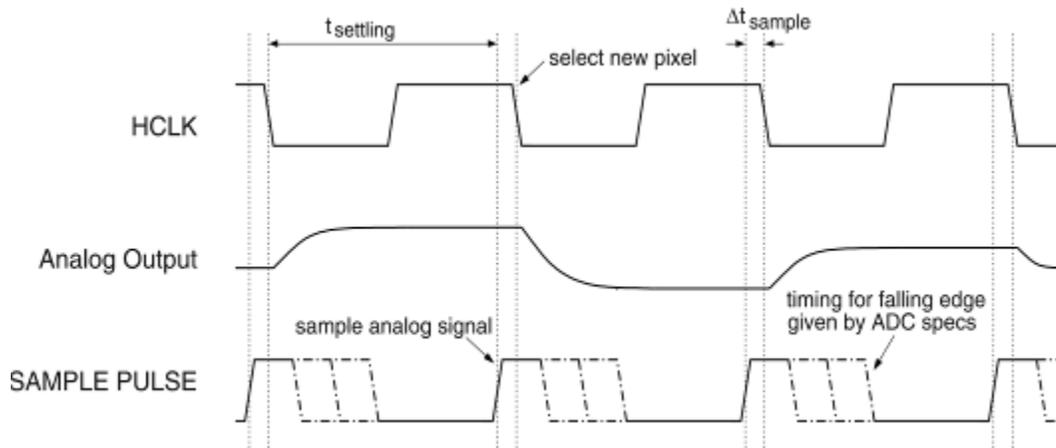


Figure 5-1: Timing for external A/D conversion

5.1.3 Full and half frequency operation of the horizontal shift register clock

In order to minimize power consumption and to reduce the crosstalk between digital clock lines and analog signal lines, the frequency of the internal horizontal shift register clock is halved compared to the pixel rate. This means a new pixel is selected every internal clock edge. Since the HAWAII-2RG multiplexer contains an internal clock divider, the user can choose whether the external HCLK signal operates at the full or half pixel rate. By default, the internal clock divider is enabled (full external clock frequency) and a new pixel is selected every falling edge of HCLK. This mode provides the most robust operation because only the cycle time but not the duty cycle of HCLK controls the readout timing. Furthermore, the external clock pattern is the same for every pixel so no odd-even effect can occur. It also means compatibility with the clock pattern used by the former HAWAII-1R multiplexer, which likewise switches to a new pixel every falling edge of the fast (horizontal) clock.

However, for some applications it can help to also half the speed of the external HCLK signal (lower clock frequency means less power and less crosstalk). For this reason, it is possible with the H-2RG multiplexer to disable the on-chip clock divider by setting the bit CLKMOD of the internal register **MiscReg** to 1. When the multiplexer is operated in this mode, the HCLK signal directly controls the horizontal shift register and a new pixel value is delivered every clock edge. Because there is now an asymmetry between odd and even pixels, it is very important that HCLK have a 50/50 duty cycle and that rise and fall times are exactly the same. Otherwise, different settling times or sampling points for odd and even pixels might occur, possibly leading to a difference in odd and even pixel values. Figure 5-2 shows the timing diagram for HCLK running at the full pixel rate or half the pixel rate, respectively.

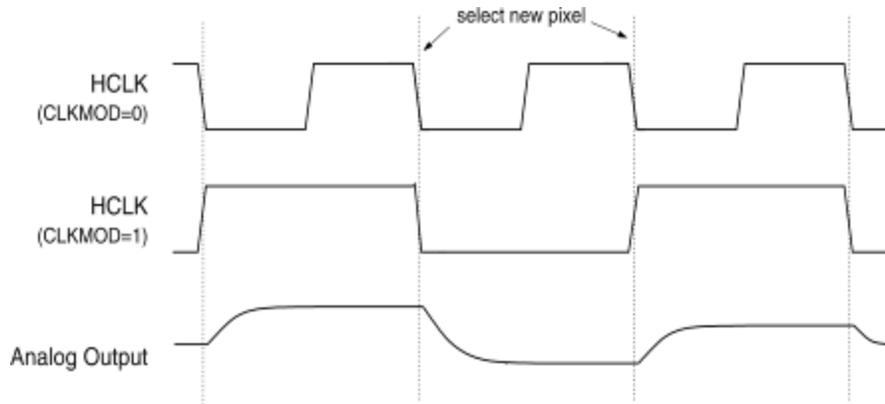


Figure 5-2: Timing diagram for HCLK running at full speed (top) or half speed (middle) compared to the pixel speed (bottom)

An additional difficulty must be handled if using the horizontal scanner without the internal clock divider (HCLK at half the pixel rate). The first HCLK edge at the beginning of a row must show a certain polarity, either rising or falling edge, depending on the current readout mode. This is to ensure that the LSYNCB signal is latched correctly and the horizontal scanner stays synchronized. Table 5.2 explains the required initial clock edges for the different readout modes. All timing diagrams throughout this section show the HCLK signal running at the pixel frequency. The corresponding timing diagrams for the second HCLK mode (HCLK at half the pixel rate) can be easily derived by replacing HCLK according to Figure 5-2 and Table 5.2.

Important: The described clock mode (HCLK running at half the pixel rate) can only be used for the slow readout operation (100 kHz)! The fast readout mode (5 MHz) requires additional internal clocks that can only be derived from HCLK running at full frequency.

Table 5.2: Polarity of first HCLK edge when starting a new row

Readout Mode	Scanning Direction	Horizontal Start Address	Horizontal Stop Address	Required Clock Edge
Full Field Mode	any	N/A	N/A	rising
Window Mode	left to right	even	any	rising
		odd	any	falling
	right to left	any	even	rising
		any	odd	falling

5.2 Normal Clocking Mode

The normal clocking mode represents the simplest way of controlling the multiplexer and reading out the pixels. Besides, it is the only mode applicable to the fast, 5 MHz operation. It requires two clock signals for the vertical (slow) scanner (VCLK and FSYNCB) and two for the horizontal (fast) scanner (HCLK and LSYNCB). Providing a negative pulse at FSYNCB or LSYNCB resets the corresponding shift register and loads a new 1 into the first register cell. VCLK or HCLK then shifts this bit through the whole shift register and consecutively select the individual rows and pixels.

5.2.1 Slow readout (100 kHz)

The slow readout mode allows the user to read out the HAWAII-2RG multiplexer at a pixel rate of 100 kHz. A 2-3 times higher rate can be achieved by increasing the bias current ($V_{biasgate}$) or accepting a less settled analog signal. The slow readout mode is fully compatible with the older HAWAII-1/2/1R multiplexers. However, since the HAWAII-2RG provides an internal clock buffer for the horizontal (fast) shift register, only one external fast clock (HCLK) is required. Hence, three of the four non-overlapped fast clocks required by the HAWAII-2 and -1R can be discarded. To simulate the clocking pattern of the HAWAII-1 multiplexer, the HAWAII-2RG horizontal scanner needs to be switched to the “one pixel per clock edge” mode (cf. Section 5.1.3) by setting the bit CLKMOD of the internal register **MiscReg** to 1.

Figure 5-3 shows a basic overview of the readout architecture used for the slow operation. It is comprised of the sensor unit cell (pixel), the vertical scanner unit cell, the horizontal scanner unit cell, and the optional output buffer. The corresponding timing diagram for the normal clocking mode can be seen in Figure 5-4. In addition to the four required clocks FSYNCB, VCLK, LSYNCB and HCLK, it contains the two digital check signals FRAMECHK and LINECHK generated by the multiplexer itself. They indicate the frame end and row end and can be used as a feedback to the external control electronics. By default, LINECHK and FRAMECHK are disabled to minimize power and glow. They can be enabled either by the external signals VTESTEN and HTESTEN or by the bits VTESTEN and HTESTEN of the internal register **GainReg**.

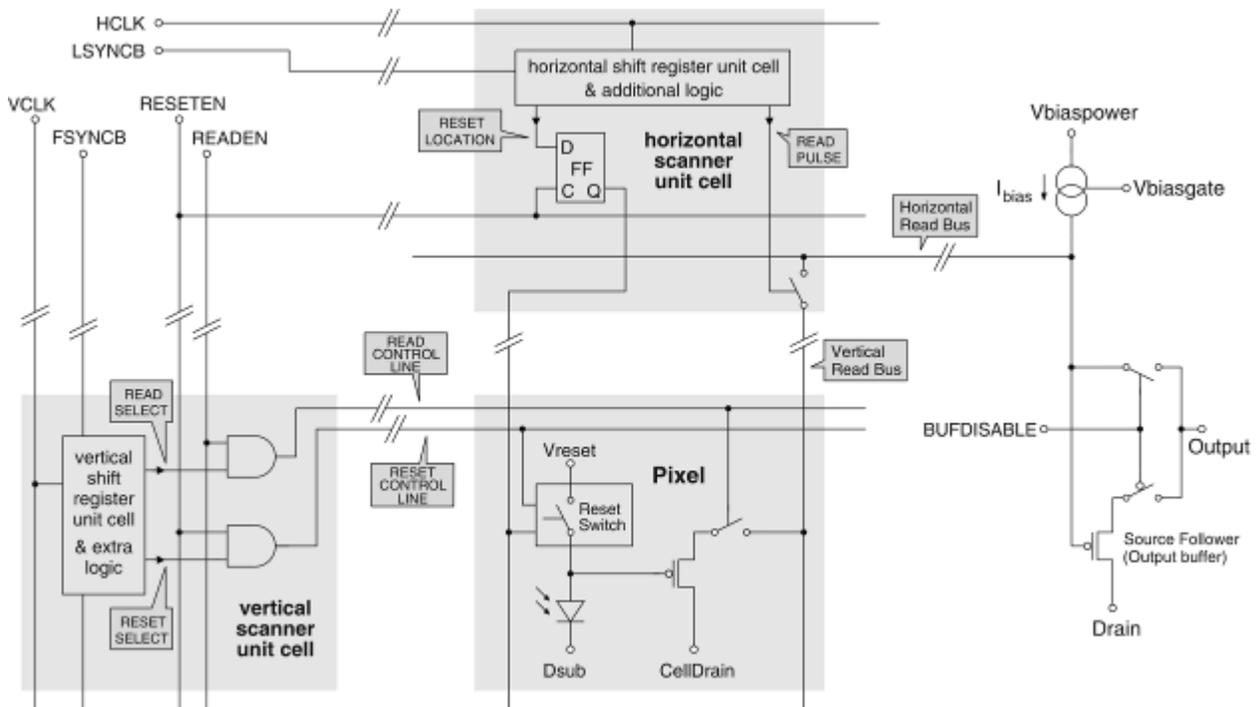


Figure 5-3: Basic readout architecture for slow mode (100 kHz) operation

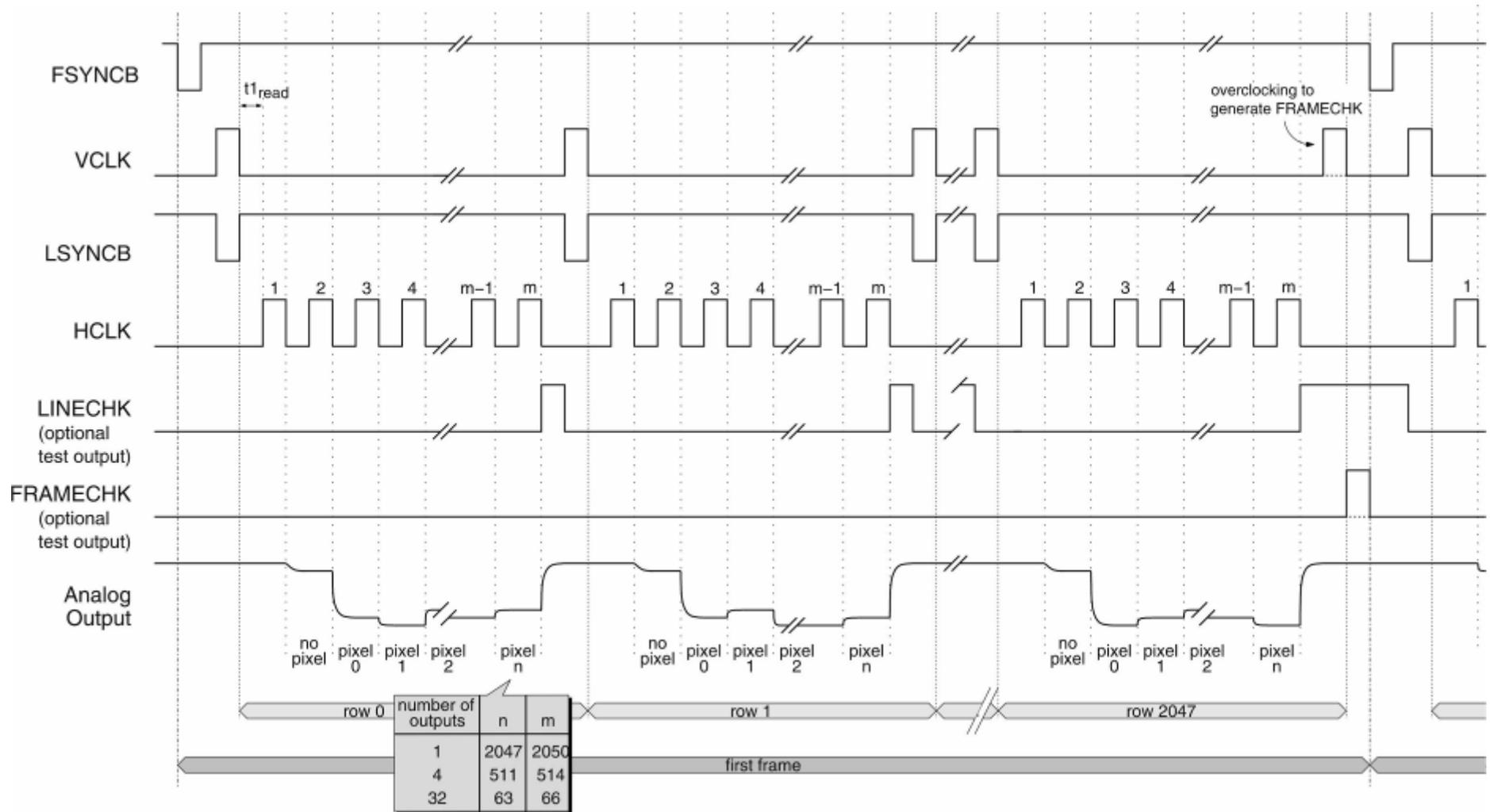


Figure 5-4: Readout timing diagram for 100 kHz operation

The two control signals RESETEN and READEN (see Figure 5-3) are not included in the timing diagram. The correct operation of RESETEN is explained in *Chapter 6: Reset Modes*. READEN can stay high during the complete readout cycle. As can be derived from Figure 5-3, these signals simply enable or disable the individual horizontal control lines used for reading or resetting the current row. In addition, a rising edge of RESETEN updates the flipflops in the horizontal scanner. The flipflops store the position of the columns that are selected for reset (only required for window operation and pixel by pixel reset). For further information on the other I/O signals (like bias voltages) see *Chapter 2: Input/Output signals and requirements*.

The analog output voltage V_{out} has a fixed offset due to the voltage drop across the source follower transistor in the pixel and, if enabled, across the output buffer transistor. Although this offset significantly depends on the actual operating conditions like bias current and temperature, a rough estimate can be given for room temperature (5 uA pixel current and 100 uA output buffer current):

$$V_{out} = V_{detector} + 900 \text{ mV (offset pixel source follower)} + 750 \text{ mV (offset output buffer)}$$

where $V_{detector}$ is the voltage at the integrating node of the detector diode. The offset increases for lower temperatures and higher bias currents. The gain of the pixel source follower as well as the output buffer is very close to 1, the combined gain of both buffers is greater than 0.95.

Although the VCLK and LSYNCB pulses coincide in the given timing diagram, they are independent and can be separated. With the falling edge of VCLK, the vertical scanner proceeds to the next row. With the falling edge of LSYNCB, the horizontal shift register is reset and is ready for a new scan. The time between the VCLK pulse and the first HCLK pulse t_{1read} depends on the applied reset pattern during the reset frame (see *Chapter 6: Reset Modes*). Since reset and readout frames should have the same timing, t_{1read} might become longer than minimum in order to match the t_{1reset} time shown in Figure 6-1 (line by line reset). The number of VCLK cycles per frame is 2048 (plus one extra clock pulse to overclock the vertical shift register if it is not immediately reset by a new FSYNCB pulse). The number of HCLK cycles per row depends on the selected output mode (1, 4 or 32 outputs) and is given in the table attached to the timing diagram. It is important to note that the first pixel value only becomes valid with the second falling edge of HCLK. This behavior is the result of an internal bus precharge, which helps reduce the external analog settling time. As a consequence, the number of HCLK cycles needs to exceed the number of pixels per row by 2.

5.2.2 Fast readout (5 MHz)

At the cost of slightly increased read noise, the HAWAII-2RG multiplexer can be read out at a pixel rate of 5 MHz allowing a maximum frame rate of 36 Hz (in 32 output mode). In this readout mode, an additional column-wise sample&hold stage plus programmable gain amplifier (column buffer) is used. This column buffer cell together with the horizontal read bus and the output buffer circuitry is shown in Figure 5-5. The external signal FASTENPAD or the bit FASTEN of the internal register **MiscReg** enable the fast readout mode and connect the individual vertical read busses to the input of the sample&hold stages. Because every vertical read bus now has its own current source providing I_{bias} for the pixel source follower, all pixels of the selected row can be sampled at the same time. Every column buffer cell contains two sample capacitors (Cap A and Cap B). The first one holds the value of the previous row and is read out through the column buffers and the horizontal scanner. The second one, at the same time as the first one is read out, samples the pixel outputs of the currently selected row. As a consequence of this architecture, there is a delay of one row time between selecting a row and seeing the corresponding pixel values at the output. The external clock signal SAMPLECLK or the bit SAMPCLK of the internal register **MiscReg** decides which capacitor is sampling and which is holding. The diagram in Figure 5-6 clarifies the overall readout timing for the fast mode operation.

Compared to the slow readout mode, a number of additional analog reference and bias voltages need to be supplied. The column buffer requires the four bias voltages V_{nbias} , V_{pbias} , V_{ncasc} and V_{pcasc} , and the fast output buffer is controlled by $V_{biasoutbuf}$. Detailed information about these voltages can be found in Section 2.2. The two reference voltages RefSample and RefColbuf are used in the sample&hold stages and allow the user to perform a level shift of the output signal over a wide voltage range.

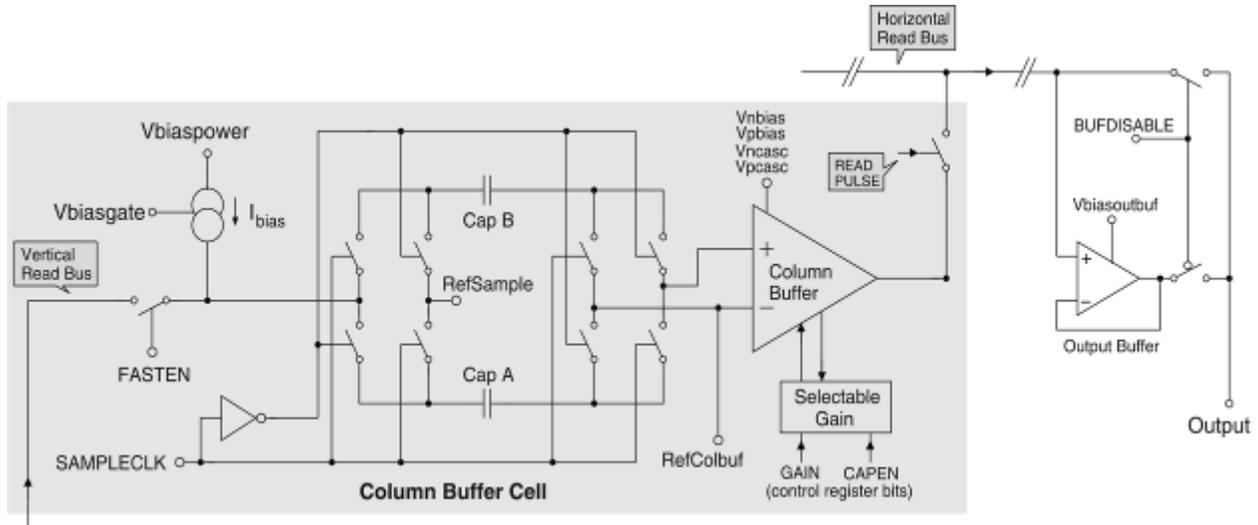


Figure 5-5: Architecture of column buffer cell for fast mode (5 MHz) operation

The sampling scheme in the column buffer cell works as follows: When SAMPLECLK is low, the right node of Cap A is connected to RefColbuf and the left node to the selected pixel via the vertical read bus. Consequently, the voltage across Cap A is $RefColbuf - V_{pixel}$ with V_{pixel} the output voltage of the pixel source follower. When SAMPLECLK goes high, the right node of Cap A gets connected to the column buffer input and the left node to RefSample. Since the voltage on Cap A does not change during this transition, the voltage V_{in} at the positive column buffer input now results in

$$V_{in} = RefSample + (RefColbuf - V_{pixel}).$$

The column buffer amplifies the difference between its positive and negative input by the selected gain. The amplifier offset is automatically calibrated in such a way that the amplifier output shows a voltage of $V_{out} = RefColbuf$, if the difference between positive and negative input is zero. With RefColbuf connected to the negative input, the voltage at the buffer output which is equal to the analog multiplexer output can be calculated:

$$\begin{aligned} V_{out} &= RefColbuf + A * (V_{inp} - V_{inn}) \\ &= RefColbuf + A * (RefSample + (RefColbuf - V_{pixel}) - RefColbuf) \\ &= RefColbuf + A * (RefSample - V_{pixel}) \end{aligned}$$

where A is the selected gain of the column buffer. Due to the negative sign of V_{pixel} , the analog output in fast mode is inverted. It needs to be noted that some constraints apply to the allowed voltage range of RefSample and RefColbuf. These constraints are explained in Section 2.2.

The column buffer gain A is controlled by the 4 GAIN bits of the internal register **GainReg** and is given by $A = GAIN + 1$. The possible range is given by $1 \leq A \leq 16$. Due to capacitor mismatch a slight gain variation on the order of ~0.1 percent can be expected across the horizontal scanner. In addition, the absolute gain value might differ from its nominal value by up to 10 percent caused by parasitic capacitance in the amplifier feedback loop. The exact values need to be obtained by measurement. The bit CAPEN in the **GainReg** register enables an additional compensation capacitor to increase the stability of the column buffer. Whether or not it is needed depends on the selected gain, the external capacitance connected to the analog output (if the internal output buffer is disabled) and the amount of ringing that can be accepted. In most cases, it should be enabled for $A = 1$ and can be disabled for $A > 1$.

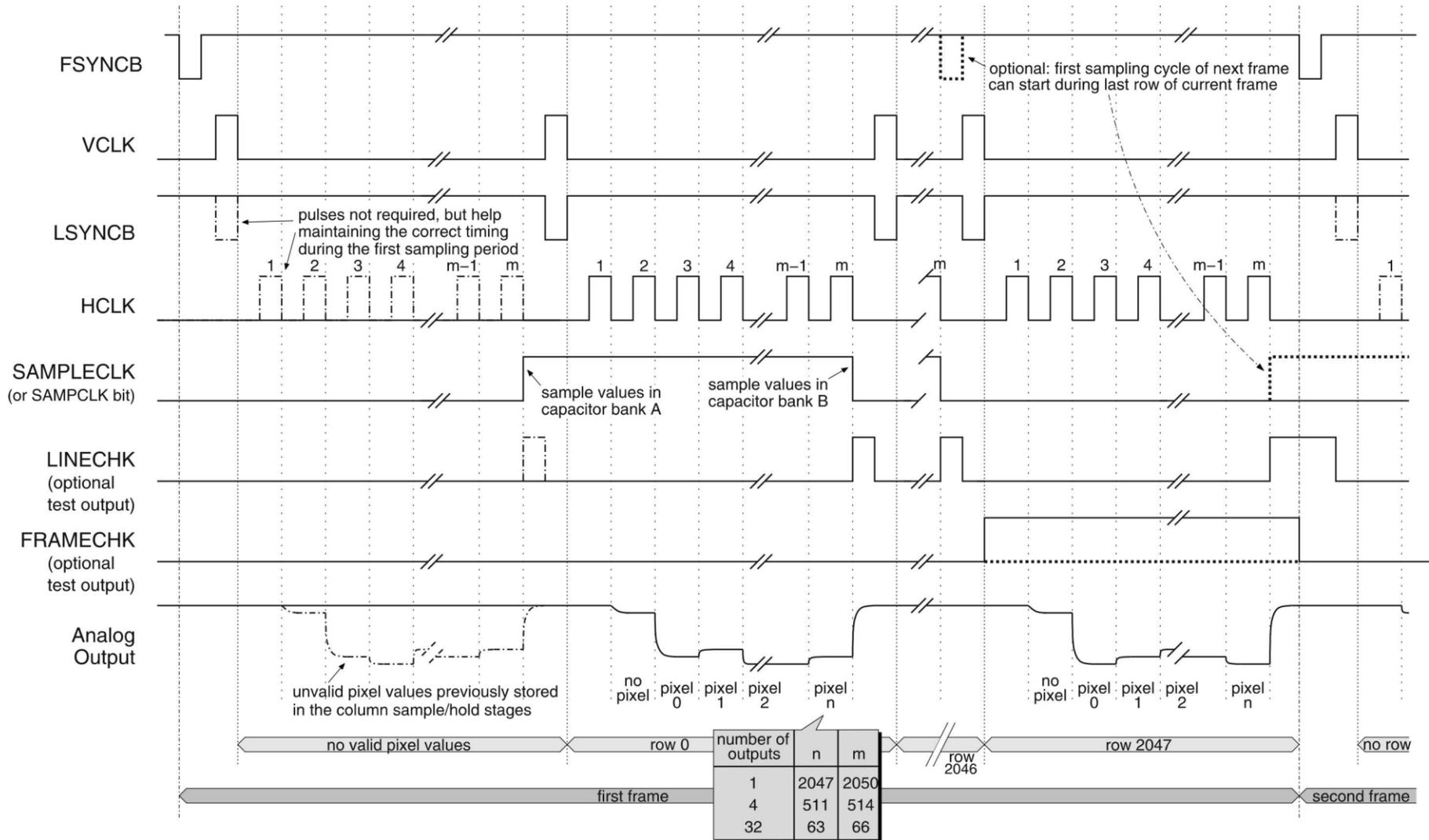


Figure 5-6: Readout timing diagram for 5 MHz operation

Except for the delay of one row between selecting a row and reading the pixel values, the timing diagram for the fast readout operation (Figure 5-6) is very similar to the one for the slow readout mode (Figure 5-4). The only additional signal is SAMPLECLK, which changes its signal level every time before proceeding to the next row (VCLK pulse) in order to store the pixel values on the sampling capacitors. During the first row of a new frame, there are no signal values stored on the capacitors (except maybe old ones from the last row of the previous frame). Therefore, it is not necessary to clock LSYNCB and HCLK during the first row, but it is still recommended to maintain equal conditions for every row of the frame. In the case where a new frame is read immediately after finishing the previous one, a new FSYNCB pulse can be applied right before the last row of the old frame. By this means, the values of the new first row will already be sampled onto the column caps when the old frame is over and the new readout can start without the delay of one row time. However, it needs to be ensured that the FSYNCB pulse does not change the timing of the last row compared to the other rows.

5.3 Enhanced Clocking Mode

The vertical and horizontal scanners can be switched to a more flexible control mode than the standard mode described in the previous section. This enhanced clocking mode enables subframe and subrow integration times as well as delay times below a frame time between two consecutive reads of the complete frame. It also allows the user to reset single pixels on the fly without the need of individually programming their addresses in window mode (see Section 6.3). In order to achieve this functionality, the meaning of the FSYNCB and LSYNCB lines has to change. They no longer reset and restart the shift register but are simply the data input of the first shift register cell. Whatever level is applied to these two signals during the falling edge of VCLK or HCLK gets inverted (LSYNCB and FSYNCB are active-low) and then clocked into the shift register. In addition, the scanner logic is no longer level sensitive but becomes edge sensitive. The term ‘edge’ refers to a transition from 0 to 1 or from 1 to 0 between the individual shift register cells. This allows the user to simultaneously define two different locations along the scanner (falling and rising edge) that can be separately used for the read or reset position. The enhanced clocking mode can be independently enabled for the vertical (slow) or the horizontal (fast) scanner.

Important: The rising and falling edge is relative to the internal clock transition within the shift register. Hence, for the active-low pulses FSYNCB or LSYNCB the “rising” edge is actually the 1 to 0 transition. Internally, these active-low clocks are inverted so activation, i.e., the transition on FSYNCB or LSYNCB from 1 to 0, is actually a 0 to 1 transition in the internal shift register.

5.3.1 Vertical Scanner

Setting the bit VMODE in the **NormalModeReg** register (full field readout) or the bit VMODWM in the **WindowModeReg** register (window readout) enables the enhanced clocking mode for the vertical scanner. Figure 5-7 shows one, of many, possible timing diagrams that can be implemented. It describes the clock pattern required to obtain a CDS (correlated double sampling) frame with an integration time of 7 row times. By varying the pulse width of FSYNCB, the integration time can be changed to any number of rows. Other readout patterns such as uncorrelated frames (reset + single reads) with random integration time or double frame reads without any reset can be easily derived from the given timing diagram. For the sake of simplicity, the horizontal scanner is still operated in normal clocking mode (see next section for enhanced clocking mode of the horizontal scanner).

Compared to the timing diagram of the normal clocking mode, Figure 5-7 contains a number of additional clock signals. The active-low VRESETB signal or the bit VRSTB in the **MiscReg** register (combined by a logical and) resets the vertical shift register. It is not necessarily required but helps to resynchronize the register cells if the history is unknown (e.g., some cells might still contain logical 1s from the previous read). The VREADEDGE signal and the bit VEDGE in the **NormalModeReg** register (combined by a logical “or”) select the edge used for controlling the read position.

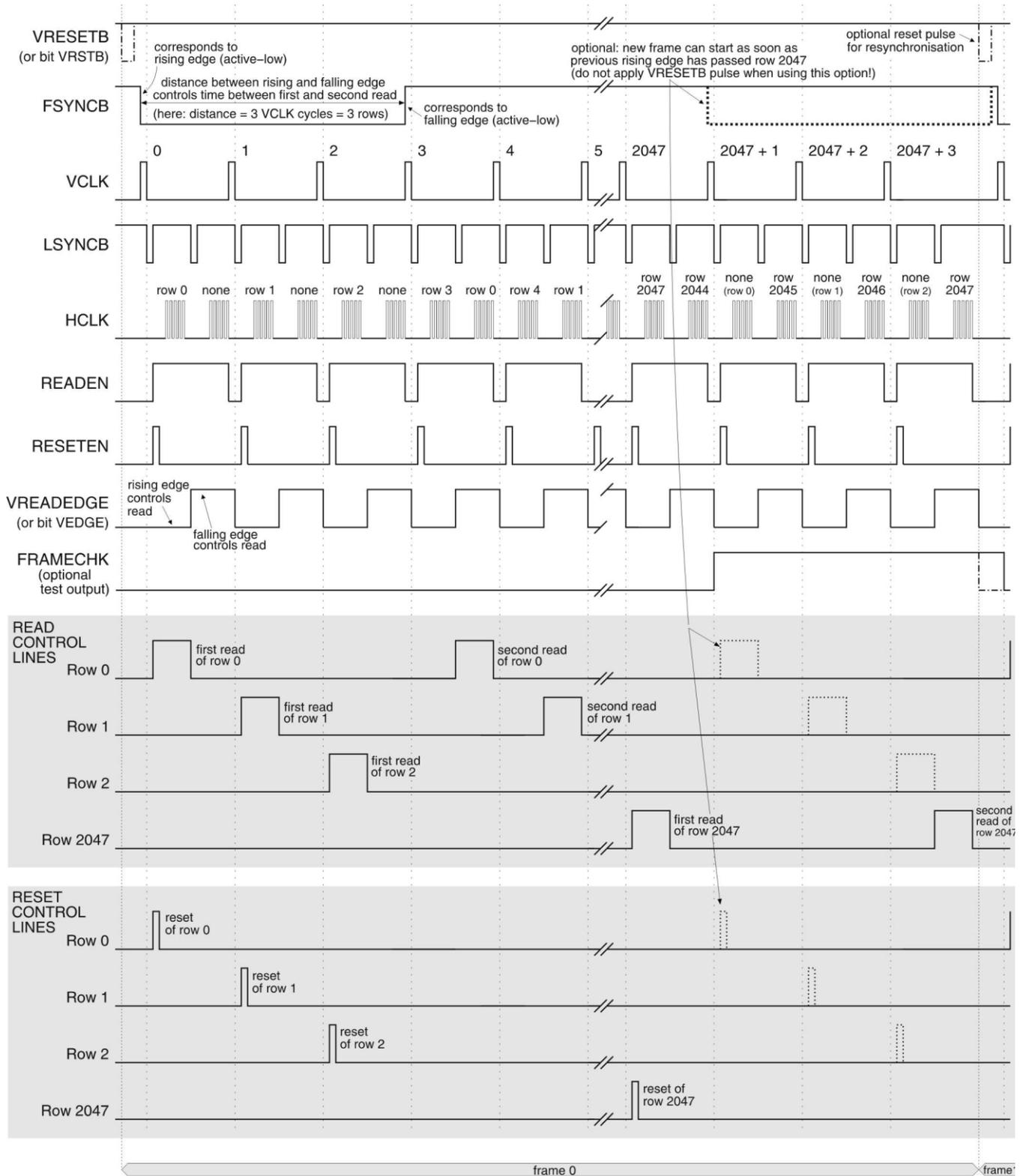


Figure 5-7: Enhanced clocking mode of the vertical scanner

A logical 0 selects the rising edge, a logical 1 selects the falling edge. The bit **RSTEDGE** in the **NormalModeReg** provides the same functionality for the reset position. It is not shown in the diagram because, for the given readout timing, it needs to be zero all the time. The additional signals **READ CONTROL LINES** and **RESET CONTROL LINES** represent the internal row selection lines for read and reset (cf. Figure 5-3). They are only shown to provide a better understanding of the readout operation.

The principle clocking pattern works as follows: After pulling **FSYNCB** down, the next **VCLK** pulse clocks the first rising edge into the register cell 0. Since **VREADEDGE** is low, this rising edge selects row 0 for read as soon as **READEN** goes high. In addition, the rising edge controls the reset position (**RSTEDGE=0**), so the next **RESETEN** pulse carries out a reset of row 0. Then, the row is read out for the first time by clocking the horizontal scanner with **HCLK**. Next, **VREADEDGE** goes high selecting the falling edge location for read. Since there is no falling edge yet, no data is read. Nevertheless, in order to maintain the correct timing, the horizontal scanner (**HCLK**) is clocked as if there was data to be read. Further pulses of **VCLK** let the rising edge proceed row by row. After 3 **VCLK** pulses, **FSYNCB** is pulled high and provides the first falling edge at row 0 after the next **VCLK** pulse. Now, a high **VREADEDGE** signal allows the second read of row 0. The reset is not active this time because **RESETEN** only pulses high when **VREADEDGE** is low, i.e., it only resets the row when activated by the rising edge of **FSYNCB**. Hence, two reads of row 0 have occurred following its reset and the reads are separated in time by the length of the **FSYNCB** pulse plus half a **VCLK** cycle.

From now on, another 2047 **VCLK** pulses are needed to finish the frame, which results in a total of 3 + 2048 pulses. If the **VRESETB** pulse is not required for resynchronization, the second frame can start while the first frame is still in progress. This is possible because a new rising edge (**FSYNCB** low) can be loaded into the shift register as soon as the previous one has left the last register cell (2047). By this means, the total number of **VCLK** pulses per frame is equal to the number of rows, which is 2048. However, the user must ensure that there are never two rising or falling edges at the same time in the shift register. This would cause two rows to be selected at the same time destroying the pixel information at the multiplexer output.

5.3.2 Horizontal Scanner

Setting the bit **HMODE** in the **NormalModeReg** register (full field readout) or the bit **HMODWM** in the **WindowModeReg** register (window readout) enables the enhanced clocking mode for the horizontal scanner. Figure 5-8 shows one example of an enhanced mode timing diagram. It describes the clock pattern required to obtain a CDS (correlated double sampling) frame with an integration time of 5 pixel times corresponding to an **LSYNCB** pulse width of 2 **HCLK** cycles. By varying the width of the **LSYNCB** pulse (allowed is any even number of **HCLK** cycles), the integration time can be arbitrarily changed to other numbers of pixel times. Other readout patterns like uncorrelated frames (reset + single reads) with random integration time or a single pixel reset scheme (see Section 6.3 under “single pixel reset without address programming”) can be easily derived from the given timing diagram. For the sake of simplicity, the vertical scanner is operated in normal clocking mode. However, there is no restriction for using both scanners in enhanced clocking mode at the same time.

Compared to the timing diagram for normal clocking mode, Figure 5-7 contains a number of additional clock signals. The active-low **HRESETB** signal or the bit **HRSTB** in the **MiscReg** register (combined by a logical AND) reset the horizontal shift register. Although **HRESETB** is not necessarily required, it helps resynchronize the register cells if the history is unknown (e.g. some cells might still contain logical 1s from the previous read or due to a possible single event upset). The **HREADEDGE** signal or the bit **HEDGE** in the register **NormalModeReg** (combined by a logical OR) selects the edge used for controlling the read position. A logical 0 selects the rising edge, a logical 1 selects the falling edge. The edge controlling the reset position cannot be chosen. It is hardwired to always be the rising edge of the shift register pattern. The additional signals **READ PULSE** and **RESET LOCATION** represent internal control lines for read and reset (cf. Figure 5-3). They are only shown to provide a better understanding of the readout operation.

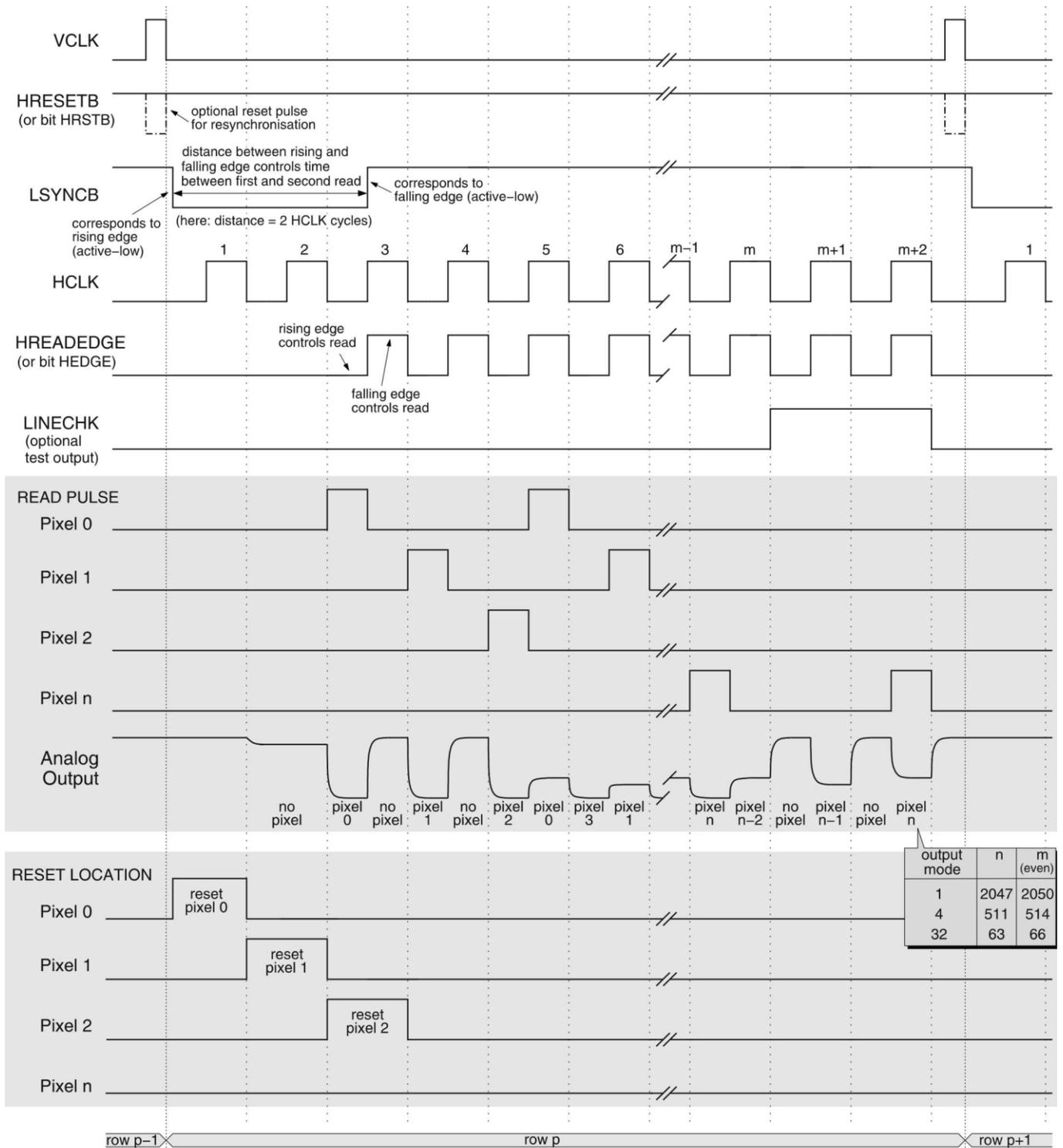


Figure 5-8: Enhanced clocking mode of the horizontal scanner

The principle clocking pattern can be described as follows: After proceeding to the next row at the falling edge of VCLK, a low LSYNCB level immediately enables the reset of the first pixel (pixel 0). At the first falling edge of HCLK, the reset pulse proceeds to pixel 1. Due to the internal precharge of the column bus, the first pixel value (pixel 0) appears at the second falling edge of HCLK. Since HREADEGE is low, its position is controlled by the rising edge of the bit pattern in the shift register. After half of the third HCLK cycle, HREADEGE goes high to let the falling edge control the read position. However, because there is no falling edge in the shift register yet, no pixel is read at this time. This falling edge is generated by the rising edge of LSYNCB, which is clocked into the shift register with the third pulse of HCLK. Again, due to the internal precharge delay, the first pixel controlled by the falling edge becomes available after the fourth HCLK pulse. As soon as HREADEGE goes high after the fourth HCLK pulse, pixel 0 again appears at the output and can be read for a second time. Hence, two reads of row 0 have occurred following its reset and the reads are separated in time by the length of the LSYNCB pulse plus half an HCLK cycle.

The pattern now moves through the horizontal scanner alternately providing first and second reads of the individual pixels. Compared to the normal clocking mode, the total number of HCLK cycles per row needs to be increased by the number of clock cycles defining the LSYNCB pulse width (here: 2 additional clock cycles). Also, if no HRESETB pulse is applied between rows, the total number of HCLK pulses needs to be even in order to maintain the internal synchronization.

Important: If using the described readout mode (alternately reading pixels at the rising and at the falling edge of the shift register bit pattern), the internal bus precharge cannot be used. For this reason, the settling time might be increased compared to the normal readout mode. To compensate for this effect, either a longer pixel readout time or a higher bias voltage for the participating buffers should be employed. This restriction does not apply if HREADEGE does not change between two consecutive pixel reads (e.g., the single pixel reset pattern without address programming in Section 6.3).

5.4 Window Readout Mode

The window mode of the HAWAII-2RG multiplexer allows the user to reset and read out any arbitrarily sized and located, rectangular sub-window. The sub-window is directly addressed, i.e., after programming the desired start and stop addresses the first window pixel can be accessed immediately. Because the various readout modes described in this and the next chapter are supported by both, the full field and the window readout mode the various timing diagrams apply to both modes. The only difference is given by the smaller number of rows or columns in window mode, so the number of HCLK and VCLK cycles needs to be adapted to the selected window size. Also, in window mode, the test outputs FRAMECHK and LINECHK indicate the end of the currently selected window and not the end of the complete shift register.

The external signals VERTWMEN and HORIWMEN or the bits VWMEN and HWMEN in the **MiscReg** register enable the window mode for the vertical and the horizontal scanner, respectively. Because both scanners contain separate shift registers for full field and window mode, the current position is not lost when switching to the other mode. For this reason, a possibly interrupted readout operation can be resumed and continued when coming back to the original mode. This capability opens the door to interleaved readout of the full field and window frames.

Although all clock and control lines are shared between full field and window mode, e.g., the same HCLK line is used for both modes, some of the settings can be chosen individually for full field or window mode. These settings are controlled by the internal registers **HoriDirReg** and **NormalModeReg** for full field operation and **WindowModeReg** for window operation.

Unlike the pixel array in full field mode, the subarray in window mode is not divided into vertical stripes corresponding to the individual outputs (cf. *Chapter 4: Output Modes*). Instead, the complete window data is always read through one single output channel no matter what output mode (1, 4 or 32 outputs) is selected. Bit WMOUTEN of the **OutputModeReg** register controls which output is used: either Output #7 (WMOUTEN

= 0) or the separate output WindowOut (WMOUTEN = 1). Because of the single output operation, the window mode requires only one bit for selecting the horizontal scanning direction (HDIRWM of the **OutputModeReg** register). This is in contrast to the full field mode where the individual outputs can have different scanning directions (**HoriDirReg** register).

The selection of the window rectangle is carried out by programming the vertical start and stop address into the registers **VertStartReg** and **VertStopReg** and the horizontal start and stop address into the registers **HoriStartReg** and **HoriStopReg**. The start address refers to the first row or column to be read and the stop address to the last row or column to be read. If the window is only one pixel wide, start and stop address will be the same.

Important: If the scanning direction is inverted (corresponding control bit set to 1), the meaning of the start and stop addresses are flipped. That means that the scan starts at the stop address and ends at the start address. But the window start and stop addresses are defined with respect to the absolute geometry of the readout and are independent of the scan direction. In other words, it needs to be ensured that the start address is always smaller than the stop address irrespective of the selected scanning direction. The vertical and horizontal start addresses always define the upper left window corner, the stop addresses always define the lower right window corner.

5.5 Guide Mode Operation

The guide mode has been originally implemented to support high frame rate guide star observations on a sub-window together with long integrating science observations on the full array. Nevertheless, the guide mode operation can be used for all other applications that require simultaneous operation of full field and sub-window readout with independently controllable reset and readout timing. Basically, the guide mode is not an additional multiplexer mode but just a combination of the previously described full field and window readout modes. It leads to an interleaved pixel pattern at the analog output which, depending on the chosen timing, contains a certain order of full field and window pixel data.

Figure 5-9 shows a possible timing diagram for the guide mode operation. It assumes that a 3 x 3 pixel sub-window has been programmed at any location in the array. Both full field and window mode are running at the slow readout speed (100 kHz) using the normal clocking mode. However, any combination of the available readout and reset modes (slow, fast, normal, enhanced, global reset, line by line reset, pixel by pixel reset) could be used as long as the specific constraints of the individual modes are observed. In the given example, the complete sub-window is read out every time a row of the full field array is finished. The VERTWMEN/HORIWMEN signals enable the window mode after every full field row and disable it again after reading one window frame.

In order to get a CDS frame of the sub-window, it is read once directly after applying the reset pulses for the individual rows and then read again after a certain integration time. In the particular case shown in Figure 5-9, the integration time amounts to the read time for one full field row plus the read time for one complete sub-window frame. Since two complete reads of the window are necessary to obtain one CDS frame, the effective frame rate is only half of the actual window frame rate. However, if CDS is not required, the window frame rate can be increased by performing a line reset right after a window row has been read. By this means, the pixels immediately start a new integration cycle and the new values can be obtained with the next window readout.

Table 5.3 shows some representative time and frame rate combinations with full field and window readouts. The first column contains the number of full field pixels read between two window reads. The second column gives the full field frame time if no window reads are carried out (standard full field readout). The right two column blocks describe the window frame rate, the increased full field frame time, and the overhead compared to the standard full field frame time for an 8 x 8 pixel sub-window and a 16 x 16 pixel sub-window, respectively.

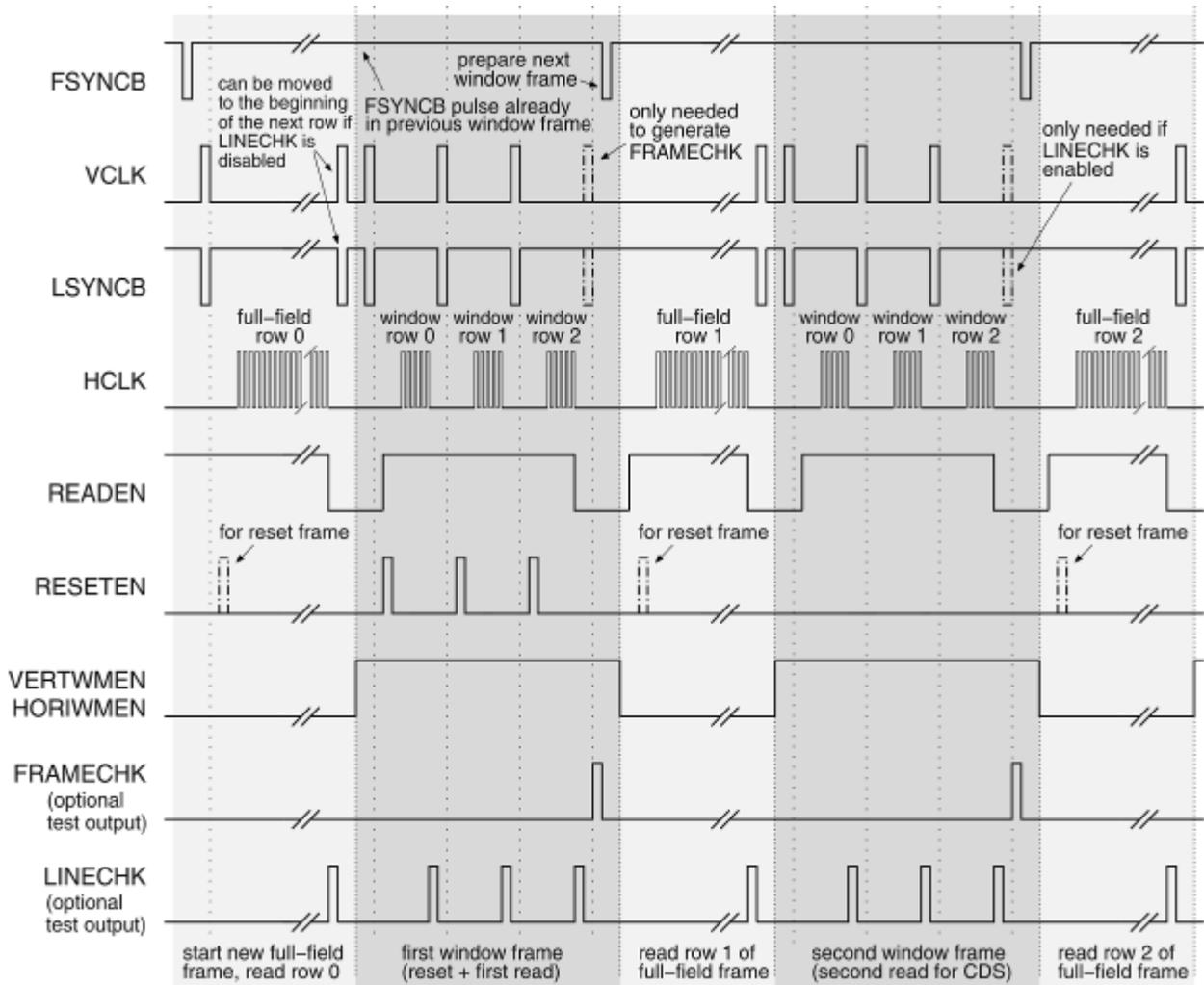


Figure 5-9: Possible timing diagram for guide mode operation

Table 5.3: Readout times for interleaved reads of full field and window array at 100 kHz pixel rate

number of pixels between two window reads	full field frame time without window	8 x 8 pixel window			16 x 16 pixel window		
		window frame rate	full field frame time	over-head	window frame rate	full field frame time	over-head
8192 (4 rows / 1 output)	42 s	12 Hz	42.4 s	1%	12 Hz	42.5 s	3.5%
2048 (1 row / 1 output)	42 s	48 Hz	43.7 s	3.9%	44 Hz	47.9 s	14%
512 (1 row / 4 outputs)	10.6 s	168 Hz	12.3 s	15.6%	124 Hz	16.5 s	56%
64 (1 row / 32 outputs)	1.36 s	680 Hz	3.0 s	122%	281 Hz	7.3 s	435%

6 Reset Modes

The HAWAII-2RG multiplexer is capable of performing three different reset schemes, all of which can be applied to the full field or window readout mode:

- **Global Reset:** All pixels are reset at the same time.
- **Line by Line Reset:** All pixels of the same row are reset at the same time.
- **Pixel by Pixel Reset:** Only one pixel is reset at a given time.

The current reset mode is selected by certain control bits of the internal registers (cf. Table 3.2). Switching between the reset modes is possible any time during operation by changing the corresponding control bits. A wait time of up to 2 μ s before starting the first reset might be necessary when enabling the global reset in window mode or when changing the window size in global reset mode. The reason for this delay is due to the global reset decoding logic that can lead to invalid pixel selections for a certain transition time.

6.1 Global Reset

Setting the GLOBAL bit in the **NormalModeReg** register or the GLOBWM bit in the **WindowModeReg** register enables the global reset scheme for the full field readout mode or the window readout mode, respectively. In full field readout mode, all 2048 x 2048 pixels are being reset while in window readout mode only the pixels inside the selected window are affected. Because the vertical and horizontal scanner can be independently switched to window mode, it becomes possible to reset all pixels in one or more rows or one or more columns by switching only one scanner to window mode. In this case, only one window dimension (horizontal or vertical) needs to be programmed while the other dimension is the total array size of 2048. The global reset in full window mode (both scanners switched to window mode) can be very useful to reset single pixels or pixel clusters, e.g., to prevent overflow in very bright areas of the scene.

The actual reset is controlled by the input signal RESETEN. Pulling RESETEN up starts the reset by turning on the reset FET in the pixel. Pulling RESETEN down stops the reset and starts the integration phase. During the global reset phase of the full array, the total capacitance at the Vreset voltage node is 2048 x 2048 x C_{pix} (capacitance per pixel). For an estimated pixel capacitance of $C_{pix} = 40$ fF, the total capacitance amounts to more than 160 nF. Depending on the external resistance in the Vreset line, the required reset time varies but should not be below 10 μ s in any case. For 16 bit performance, a reset time of at least 12 RC time constants (external resistor and internal plus external capacitance) is recommended.

6.2 Line by Line Reset (default)

The line by line reset scheme represents the most commonly used reset pattern. It is the only one supported by the old HAWAII-1/2/1R multiplexers. All pixels in a row are being reset together. Again, a high level at the input signal RESETEN starts the reset, a low RESETEN signal stops the reset. The vertical scanner, which selects the actual row to be reset, can be operated in two different clocking modes: *normal* and *enhanced*. The bits VMODE in **NormalModeReg** and VMODWM in **WindowModeReg** select the particular clocking mode for full field operation and window operation, respectively.

Normal Clocking Mode: In normal clocking mode, the row currently selected for read is also selected for reset and is determined by the location of the digital 1 in the vertical shift register. Figure 6-1 shows an example timing diagram for two different clocking options for the RESETEN signal. Option A provides only a short RESETEN pulse at the beginning of each row in order to allow reading the individual pixel reset values during the same row period. Option B holds RESETEN high for the complete reset frame. In this case, there is less switching in the multiplexer during the reset phase, but the delay between the reset and the first read of the actual pixel values is at least one frame time.

In principal, it is possible to clock quickly through the vertical scanner during the reset frame. However, in order to assure equal times between the reset and the read phase for all pixels, it is recommended one uses the same clock pattern for readout and reset. In particular, it is important that the times $t1_{reset}$ and $t1_{read}$ (see Figure 6-1 and Figure 5-4) should be the same for read and reset frame. If the pixel values are not to be read during the reset frame, the signals LSYNCB and HCLK are not necessarily required (as long as the timing of all other clocks is maintained). Also, the READEN signal can stay low during the reset frame in order to save power (all pixel source followers disabled).

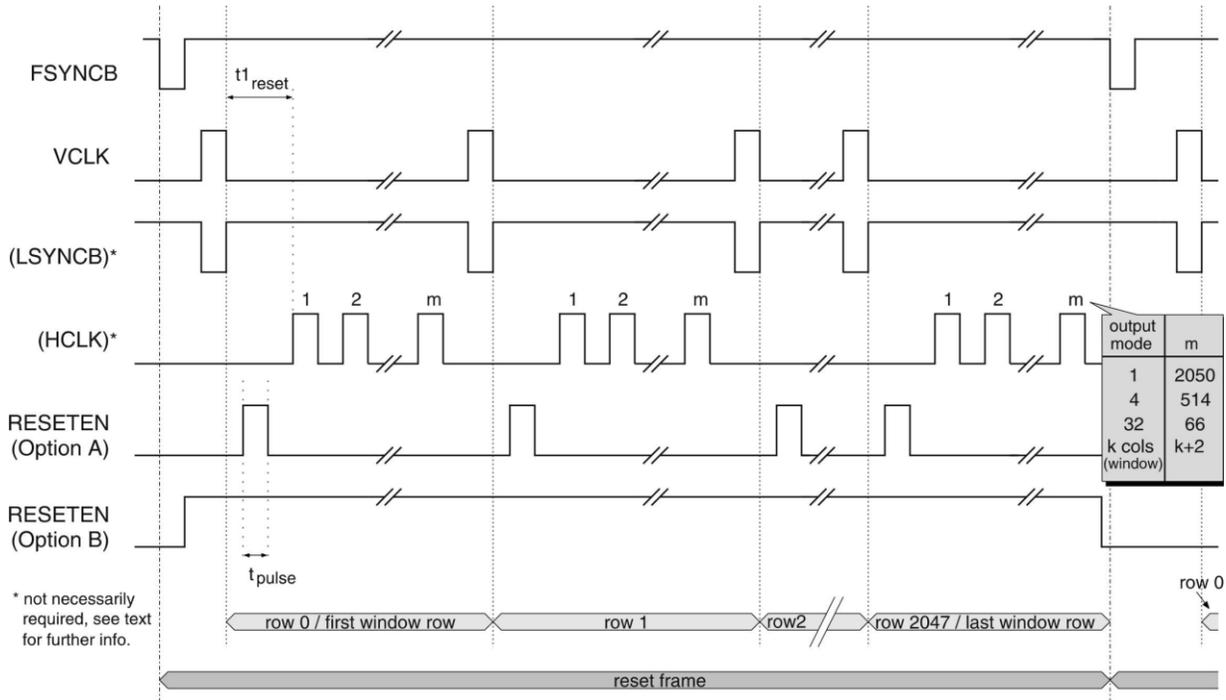


Figure 6-1: Timing diagram for line by line reset operation

Enhanced Clocking Mode: The enhanced clocking mode of the vertical scanner has been implemented to enable integration times shorter than a frame time. It allows resetting a row, reading it once and then reading it again (for CDS purposes) after a certain number of row times. While this row is integrating, other rows can be reset and read to decrease the overall readout time. Section 5.3.1 describes this readout scheme and its associated timing diagram in more detail. In normal mode, the vertical scanner is level sensitive, i.e., the current row is determined by the shift register cell containing a logical 1. In enhanced mode, the scanner becomes edge sensitive, i.e., the selected row is determined by the transition from 1 to 0 or 0 to 1. By feeding different numbers of 1s into the vertical register, the distance between the two edges can be changed. The bits RSTEDGE in **NormalModeReg** and REDGWM in **WindowModeReg** select which of the two edges will be used for reset.

For the normal as well as for the enhanced clocking mode, the reset pulse width t_{pulse} of RESETEN depends on the external resistor in the Vreset line. Together with the internal capacitance of about $2048 \times C_{pix} = 80$ pF, the RC time constant can be calculated. Usually, a reset pulse of 10 μ s or less should be sufficient.

6.3 Pixel by Pixel Reset

The pixel by pixel reset scheme allows the user to reset individual pixels. The two major advantages of this reset mode are the possibility of achieving integration times shorter than a row time and the ability to obtain the exact same time between reset and read for every pixel. With a row based or global reset scheme, the time between reset and read varies from pixel to pixel, which might limit the dynamic range under certain conditions. Due to the different readout architecture of the 5 MHz high speed outputs, the two advantages of the pixel by pixel reset scheme do not apply. Therefore, the pixel by pixel reset can only be enabled when using the slow readout mode (100 kHz).

Setting the bits HMODE in **NormalModeReg** (full field mode) or HMODWM in **WindowModeReg** (window mode) switches the horizontal scanner from *normal clocking mode* to *enhanced clocking mode* and enables the pixel by pixel reset scheme. In normal mode, the horizontal scanner is level sensitive, i.e., the current column is determined by the shift register cell containing a logical 1. In enhanced mode, the scanner becomes edge sensitive, i.e., the selected column is given by a transition from 1 to 0 or 0 to 1. Section 5.3.2 contains a detailed description and the corresponding timing diagram of the enhanced readout mode. Unlike the enhanced readout mode of the vertical scanner, the horizontal scanner does not allow the user to choose which edge is used for reset. Instead, it is always the 0 to 1 transition (rising edge) that determines the pixel currently being reset. When operating the multiplexer in pixel by pixel reset mode, the signal RESETEN can be kept high permanently. Only the pixel currently selected by the vertical (row) and horizontal (column) scanner will be reset.

Important: The rising and falling edge is relative to the internal clock transition within the shift register. Hence, for the active-low pulse LSYNCB the “rising” edge is actually the 1 to 0 transition. Internally, this active-low clock is inverted so activation, i.e., the transition on LSYNCB from 1 to 0, is actually a 0 to 1 transition in the internal shift register.

Single pixel reset without address programming

In addition to the clocking scheme shown in Section 5.3.2, the enhanced clocking mode of the horizontal scanner offers another interesting possibility. It allows the user to reset single pixels (e.g. to prevent overflow) during the normal readout procedure without the need of programming the window addresses. Figure 6-2 shows the corresponding timing diagram. The READEN signal is not shown, but should be enabled during the whole readout cycle. The pixel value is read at the falling edge (1 to 0 transition), which has to come first. This means bit HEDGE in **NormalModeReg** (full field mode) or bit HEDGWM in **WindowModeReg** (window mode), respectively, has to be set to 1. The same pixel can be reset at the rising edge (0 to 1), which is delayed by a certain amount of clock cycles, by pulling RESETEN high. This delay is given by the number of zeros fed into the horizontal scanner and can be adjusted to the evaluation time of the external electronics. Hence, “on-the-fly” reset decisions can be made on a pixel by pixel basis to prevent pixels from saturating. Due to the internal multiplexer architecture, the delay needs to be an even number of clock cycles. The example shown in Figure 6-2 assumes a latency of 4 pixels between read and reset requiring a LSYNCB pulse width of 6 clock cycles.

The READ PULSE, RESET LOCATION and RESET PULSE signals represent internal control signals and are shown only for clarification (cf. Figure 5-3). The READ PULSE signal enables a pixel for read. The RESET LOCATION signal determines the current pixel for reset, but does not perform the reset. The RESET PULSE signal finally carries out the actual reset and is the result of a logical AND of the RESETEN and the RESET LOCATION signals.

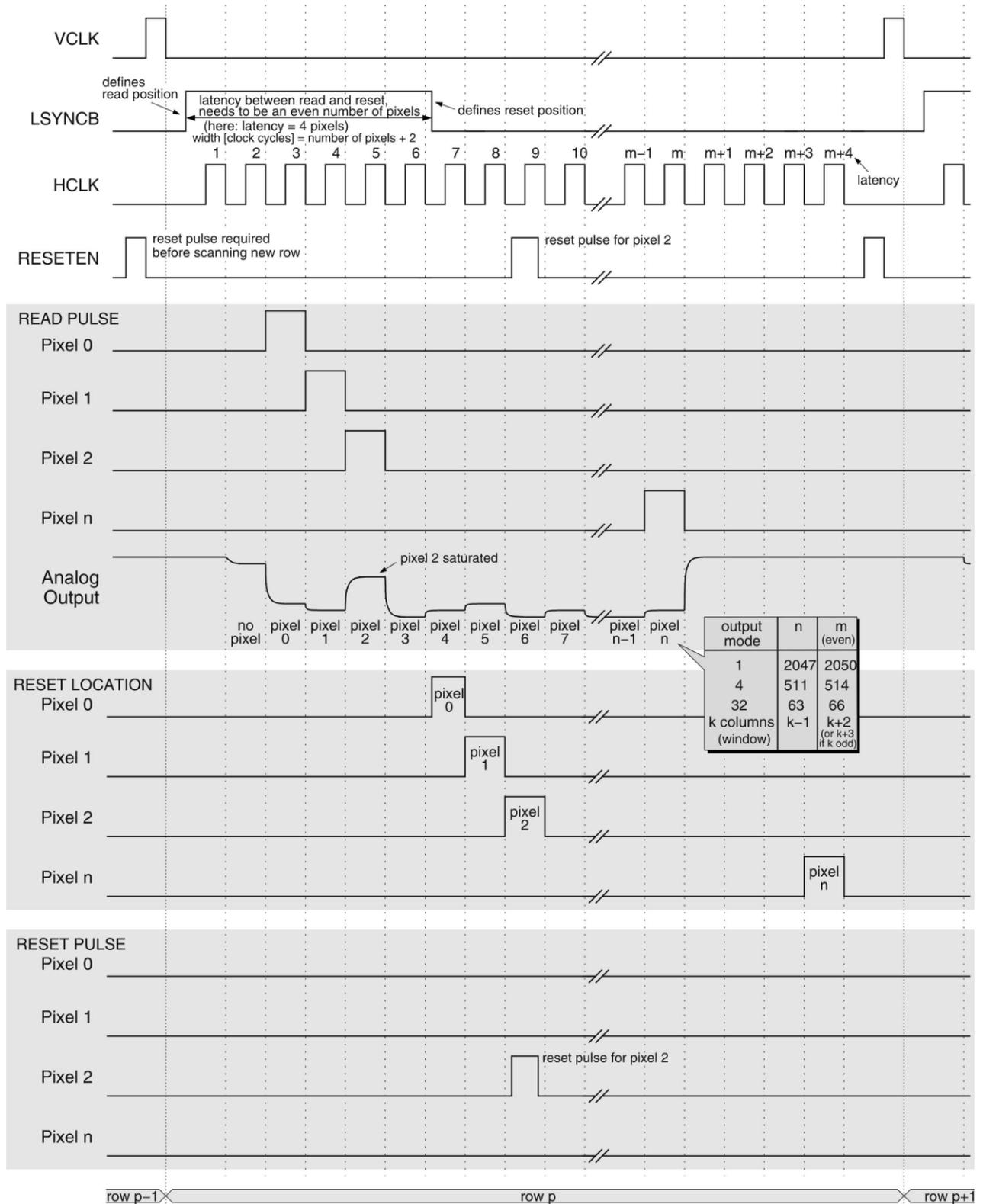


Figure 6-2: Timing diagram for resetting single pixels without programming the pixel address.

Unlike the other readout modes, this mode requires that every horizontal shift register cell contains a logical 1 after finishing a row and before starting a new row. Therefore, the horizontal scanner should not be reset between rows, which would set all shift register cells to zero. Furthermore, it is essential that the total number of clock cycles per row is even. This ensures that the horizontal scanner always starts with the same internal clock phase. For synchronization purposes, one horizontal scanner reset should be performed at the beginning of a new frame using the external HRESETB signal or the bit HRSTB of the internal register **MiscReg**. After the reset, the shift register cells need to be refilled with logical 1s (= LSYNCB low) before the actual frame readout can start. It is also important that a short reset (RESETEN) is performed between two subsequent rows in order to reset the vertical reset control lines.

7 Reference Pixels

In order to track possible bias or temperature drifts, the HAWAII-2RG provides a number of different reference pixels and readout options. In contrast to the standard active pixels, the reference pixels are not connected to detector photodiodes. Instead, they contain a simple capacitor C_{pix} whose capacitance is similar to the detector capacitance. One capacitor node is connected to D_{sub} , the other node is connected to the internal pixel node. The circuit diagram of the reference pixels is shown in Figure 7-1.

7.1 Embedded Reference Pixels

The normal detector array of 2048 x 2048 pixels contains 8 rows and 8 columns of reference pixels arranged in blocks of 4 rows/columns around the array border. This means, rows 0 – 3 and 2044 – 2047 as well as columns 0 – 3 and 2044 – 2047 are comprised of reference pixels, while the remaining inner core (rows and columns 4 – 2043) is comprised of active pixels. The reference capacitance C_{pix} is 40 fF for all reference pixels. However, the total pixel capacitance will be about 50% higher due to the additional parasitic capacitances (source follower, reset switch, etc.). Since these reference pixels are included in the main array, their readout values will be embedded in the normal data stream. They can either be evaluated immediately or be stored together with the active pixels for later analysis.

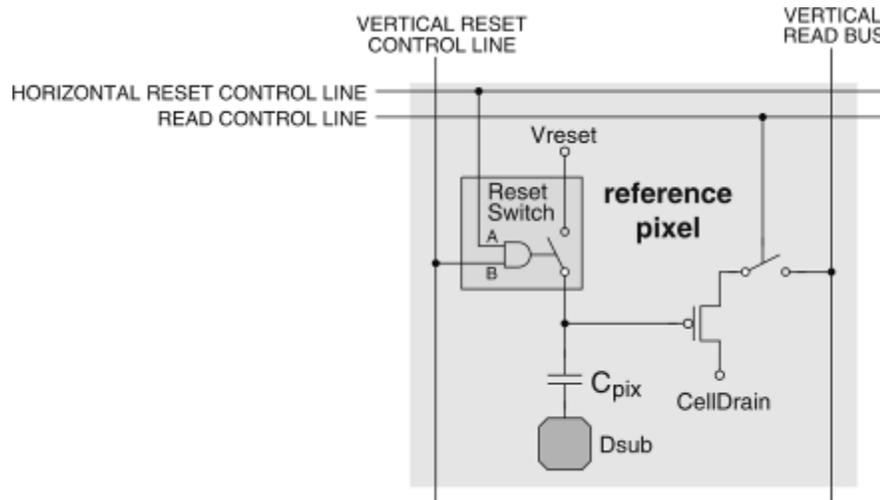


Figure 7-1: Circuit diagram of the reference pixel

7.2 Separate Reference Output

In addition to the embedded reference pixels, a separate reference output has been implemented. Since it is a completely independent output channel, it can be used in parallel with the normal output channels to, for instance, perform a fully differential readout. Please refer to Section 2.3 for further information on the different output configurations of the RefOutA/B pads. The reference signal for the separate reference output is derived from a single pixel with a capacitor of $C_{pix} = 40$ fF. This pixel is shown in Figure 7-2 together with some selection switches for controlling the specific operation mode.

In order to use the reference output, it has to be enabled by setting the bit REFPIXEN of the internal **OutputModeReg** register. In addition to connecting the pixel to the readout line, this bit also powers up the appropriate output buffer (slow, fast, buffered or non-buffered). The selected buffer can be automatically disabled during blanking times. See Section 8.3 for a description of the corresponding power down options.

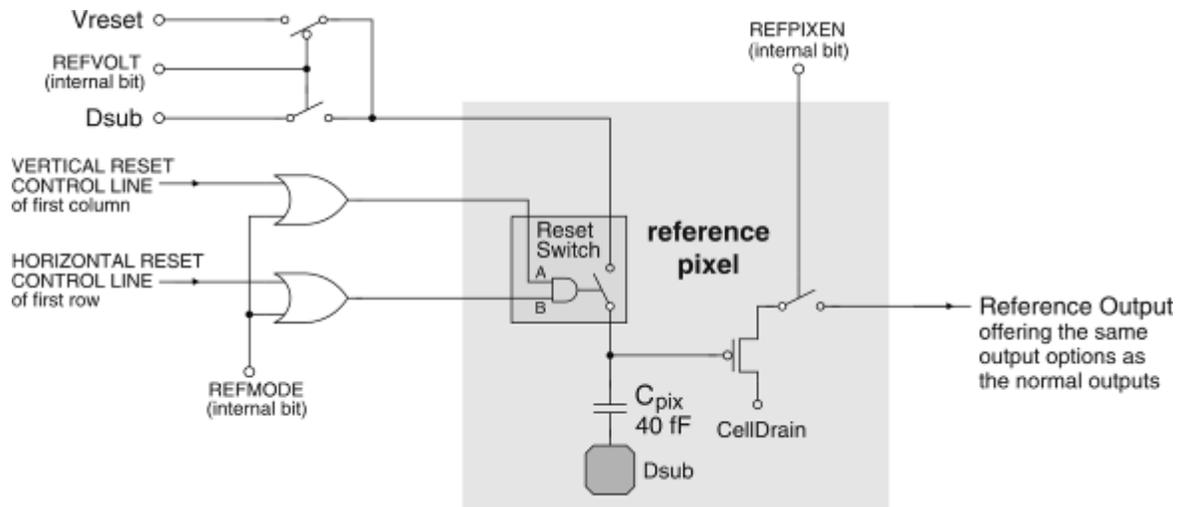


Figure 7-2: Configuration of the reference pixel for the separate reference output

The bit REFMODE of the internal **OutputModeReg** register controls the pixel operation mode. If it is 0, the pixel is treated as a normal array pixel. It is reset every time the upper left array pixel is reset (location 0,0). Between two resets, the pixel node is floating and will move slightly due to leakage currents in the connected transistors. If REFMODE is 1, the pixel stays in the reset state all the time because the pixel node is permanently connected to the applied reset voltage. This voltage can be selected to be either Dsub or Vreset depending on the bit REFVOLT of the internal **OutputModeReg** register. REFVOLT = 0 selects Vreset, REFVOLT = 1 selects Dsub.

Although the reference pixel is basically permanently connected to the reference output, there is a slight difference in how the reference channel works at the fast (5 MHz) readout speed. Because it should reflect the conditions of the normal output channels as much as possible, the reference channel also uses the column sample&hold stage plus column buffer when operated in the fast readout mode. As a consequence, there is no permanent connection between pixel and output pad. Instead, a new reference value is sampled with every level change of the SAMPLECLK signal and then held for the remaining readout time of the row.

7.3 Separate Row of Reference Pixel

An additional row of reference pixels with alternating capacitor values of $C_{pix} = 10, 20, 40$ and 80 fF is located outside the regular pixels at the top end of the array (see Figure 7-3). Once it is enabled by the bit REFROW of the internal **OutputModeReg** register, it is treated as a regular row that can be controlled and read by the standard clocking schemes of the horizontal scanner. It is used only for diagnostic purposes in order to examine the effect of different capacitance values.

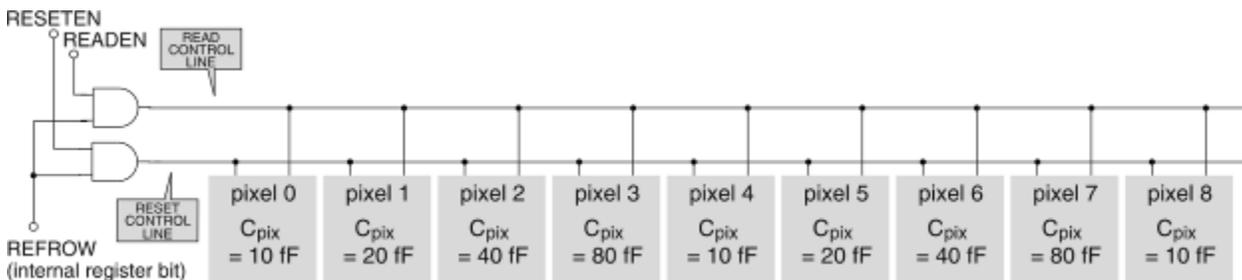


Figure 7-3: Block diagram of the additional reference row located on top of the pixel array

8 Power Down Control

For maximum power efficiency, it is important that the individual on-chip components like amplifiers or buffers are powered down when they are not used. The HAWAII-2RG offers a number of automatic power down modes for switching off individual components. In some cases, the amplifiers are simply turned off by overclocking the shift registers; in other cases, they are powered down by certain control signals. The following three sections describe the different power down properties for the slow, the fast and the separate readout.

8.1 Slow Readout Mode (100 kHz)

The slow readout operation represents the simplest mode with respect to the power down properties. The only two components consuming a quiescent current are the pixel source follower and, if enabled, the output source follower. Since the connection between the pixel source follower transistor and its current load is interrupted as soon as the horizontal scanner is reset or overclocked, or once the READEN signal goes down, the pixel buffer can easily be turned off at the end of each row. If the user needs to keep the source follower on, e.g., for a more homogeneous operation, simply do not overclock the horizontal shift register and keep the last column selected.

The same situation applies to the optional on-chip output source follower. It is automatically disabled when all the pixel source followers are disabled. The reason is that the internal current source of the pixel source follower pulls up the horizontal readout bus to vdda. This bus controls the gate of the output buffer transistor and turns it off when reaching the level of vdda. The output node becomes high-ohmic at this point.

8.2 Fast Readout Mode (5 MHz)

When switching to the fast readout operation, the situation changes for powering-down the unused stages. First, all pixels in the selected row are connected to the individual column busses at the same time. As a consequence, the pixel source followers are not turned off by overclocking or resetting the horizontal scanner. Instead, they can be only disabled by pulling down the READEN signal or by overclocking or resetting the vertical scanner (= deselecting all rows). Second, the fast readout mode requires one additional amplifier stage: the column buffers. Since they are active only during the readout of the pixels in the corresponding column, they are automatically turned off as soon as the horizontal scanner is overlocked or reset.

The most complicated component in terms of power down properties is given by the output buffer for fast mode operation. Once the buffered fast output option is selected, this amplifier can only be disabled by actively controlling its power down signal. To do so, there are basically two different options which can be applied to the full field as well as to the window mode.

The first option turns off the buffer as soon as the LINECHK signal becomes high at the end of a row. This option is controlled by the bit PDBUF0 (full field mode) and the bit PDBUF2 (window mode) of the internal **PowerDownReg** register. For using this power down mode in window operation, the LINECHK output has to be enabled (see LINECHK in Section 2.4). In full field mode, the LINECHK output does not need to be turned on.

The second option disables the output buffers when a reset of the horizontal scanner is performed. This means either a low LSYNCB signal, if operating in normal clocking mode, or a low HRESETB signal in any clocking mode (cf. Sections 5.2 and 5.3.2). This option is controlled by the bit PDBUF1 (full field mode) and the bit PDBUF3 (window mode) of the internal **PowerDownReg** register.

Whatever power down option is selected, the output buffers get powered up again once the LSYNCB signal goes down to start a new line. Exception: If the second option is selected and horizontal scanner is operated in the normal clocking mode, the output buffers are not enabled until the negative LSYNCB pulse is over. Of course, the fast output buffers can also be controlled by the external BUFDISABLE signal or the

corresponding internal control bits (cf. Section 2.3), which allow the user to disable both internal automatic power down options.

8.3 Separate Reference Output

Unlike the previously described behavior of the internal buffers in slow and partly in fast mode, the reference channel does not go into a power down state by simply overclocking or resetting the horizontal scanner. The separate reference output is independent of the scanner status. Therefore, the implementation of the reference output follows the same concept used for the fast output buffers: it can be actively powered down in two different ways. Both options apply to the slow (100 kHz) as well as to the fast (5 MHz) readout speed.

The first option turns off the reference channel as soon as the LINECHK signal goes high at the end of a row. This option is controlled by the bit PDREF0 (full field mode) and the bit PDREF2 (window mode) of the internal **PowerDownReg** register. When using this power down mode in slow and fast window operation or in slow full field operation, the LINECHK output has to be enabled (see LINECHK in Section 2.4). In fast full field mode, the LINECHK output does not need to be turned on.

The second option disables the reference channel when a reset of the horizontal scanner is performed. This means either a low LSYNCB signal, if operating in normal clocking mode, or a low HRESETB signal in any clocking mode (cf. Sections 5.2 and 5.3.2). This option is controlled by the bit PDREF1 (full field mode) and the bit PDREF3 (window mode) of the internal **PowerDownReg** register.

Whatever power down option is selected, the reference channel is powered up again once the LSYNCB signal goes down to start a new line. Exception: If the second option is selected and horizontal scanner is operated in the normal clocking mode, the reference output is not enabled until the negative LSYNCB pulse is over. If it is desired to never power down the reference channel, simply disable both control options. In this case, it can only be turned off by disabling the reference output completely (see bit REFPIXEN in Section 7.2).

Appendix

A. I/O Signal Table

Table A.1: Hawaii-2RG I/O signals

Signal Name	Direction	Type	Level [V]	Default	Usage	Pad Count	100 kHz	5 MHz	Window	Other
gnd, gnda	input	power	0	-	Power supply	2	2	2		
vdd, vdda	input	power	3.3	-	Power supply	2	2	2		
sub	input	power	0	-	Multiplexer substrate	1	1	1		
Dsub	input	bias	0 - 1	-	Detector substrate	1	1	1		
Vreset	input	bias	0 - 1	-	Detector reset voltage	1	1	1		
Celldrain	input	power	0 (or > 0)	-	Drain node of pixel source follower	1	1	1		
Drain	input	power	0 (or > 0)	-	Drain node of output source follower	1	1	1		
Vbiaspower	input	power	3.3 (or < 3.3)	-	Source node of current source for pixel source follower	1	1	1		
Vbiasgate	input	bias	~ 2.4	-	Bias of current source for pixel source follower	1	1	1		
RefColbuf, RefSample	input	ref.	0.5 - 2.0	3.3 3.3	Reference voltages for column sample&hold stages (5 MHz)	2		2		
Vnbias	input	bias	~ 0.85	0	Bias for 5 MHz column buffers	1		1		
Vncasc	input	bias	~ 1.2	0	Bias for 5 MHz column buffers	1		1		
Vpbias	input	bias	~ 2.35	3.3	Bias for 5 MHz column buffers	1		1		
Vpcasc	input	bias	~ 2.0	3.3	Bias for 5 MHz column buffers	1		1		
Vbiasoutbuf	input	bias	~ 0.85	0	Bias for 5 MHz output buffers	1		1		
OutputA, OutputB	Output	analog	0 - 3.3	-	Analog output pads (two per channel)	32				
RefOutA/B	Output	analog	0 - 3.3	-	Reference outputs	2	n	n		
WindowOutA/B	Output	analog	0 - 3.3	-	Window mode outputs (guide mode)	2				
FSYNCB	input	digital	0 / 3.3	-	Frame Sync (starts slow shift reg.) / Data In (serial interface)	1	1	1		
VCLK	input	digital	0 / 3.3	-	Slow (vertical) shift register clock / Data Clk (serial interface)	1	1	1		
VRESETB	input	digital	0 / 3.3	3.3	Reset slow shift register	1				1
LSYNCB	input	digital	0 / 3.3	-	Line Sync (starts fast shift register)	1	1	1		
HCLK	input	digital	0 / 3.3	-	Fast (horizontal) shift register clock	1	1	1		
HRESETB	input	digital	0 / 3.3	3.3	Reset fast shift register	1				1
READEN	input	digital	0 / 3.3	3.3	Enable row selection for read	1				1
RESETEN	input	digital	0 / 3.3	-	Enable row selection for reset	1	1	1		
VERTWMEN	input	digital	0 / 3.3	0	Enable vertical window mode	2			2	
HORIWMEN	input	digital	0 / 3.3	0	Enable horizontal window mode	2				
VREADEGE, HREADEGE	input	digital	0 / 3.3	0	Select which edge of FSYNCB/LSYNCB is used for read	2				2
SAMPLECLK	input	digital	0 / 3.3	0	Column buffer sample clock for 5 MHz operation	1		1		
CSB	input	digital	0 / 3.3	3.3	Chip Select (serial interface)	1			1	
DATACLK	input	digital	0 / 3.3	0	Data Clock (serial interface)	1			(1)	
DATAIN	input	digital	0 / 3.3	3.3	Data Input (serial interface)	1			(1)	
DATAOUT	output	digital	0 / 3.3	-	Data Output (serial interface)	1				1
MAINRESETB	input	digital	0 / 3.3	3.3	Reset serial interface and on-chip mode registers	1	1	1		
VTESTEN, HTESTEN	input	digital	0 / 3.3	0	Enable vertical/horizontal test output (end of register)	2				2
FRAMECHK, LINECHK	output	digital	0 / 3.3	-	Vertical / horizontal test outputs (end of register)	2				2
MODECTRL1, MODECTRL2	input	digital	0 / 3.3	0, 0	Select output mode (1, 4, 32 outputs)	2				2
BUFFERDISABLE	input	digital	0 / 3.3	0	Disable on-chip buffers	1				1
FASTENPAD	input	digital	0 / 3.3	0	Enable fast mode (5 MHz)	1				1
Temperature Pads	in/out	analog	0 - 3.3	-	Temperature Sensors	4				4

Signal Name	Direction	Type	Level [V]	Default	Usage	Pad Count	100 kHz	5 MHz	Window	Other
HCLK1, HCLK1B, HCLK2, HCLK2B	input	digital	0 / 3.3	-	Backup clock input for fast (horizontal) shift register clock in full field mode (bypass on-chip clock buffers)	4				(4) backup
HCLKWM1, HCLKWM1B, HCLKWM2, HCLKWM2B	input	digital	0 / 3.3	-	Backup clock input for fast (horizontal) shift register clock in window mode (bypass on-chip clock buffers)	4				(4) backup
TOTAL						124	17+ n	24 + n	3 (5)	18 (26)

B. I/O Pad Locations

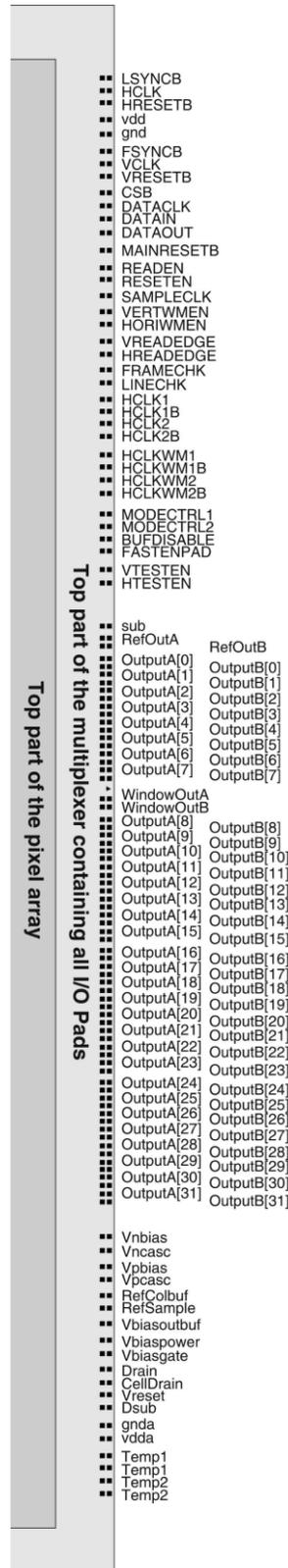


Figure B.1: Top part of the HAWAII-2RG (rotated) showing all I/O Pad locations (2 pads per signal)

C. Technical Specifications

Resolution	Complete array	2048 x 2048
	Active pixels (light sensitive)	2040 x 2040 (centered)
	Reference pixels	4 outer rows/columns on all 4 sides
Pixel Dimensions	Width	18 μ m
	Length	18 μ m
Die Dimensions	Width (horizontal)	Max. 38.86 mm (1 mm extension to the active area on both sides) Min. 37.73 mm (0.65 mm extension on the left and 0.22 mm extension on the right side)
	Length (vertical)	Max. 40.07 mm (1 mm extension on the bottom and 2.21 mm extension on the top side) Min. 39.27 mm (0.20 mm extension on the bottom and 2.21 mm extension on the top side)
Technology		0.25 μ m CMOS
Pixel Rate	Slow mode	Nominal 100 kHz
	Fast mode	Nominal 5 MHz
Power Supply	Analog (vdda)	3.3 V
	Digital (vdd)	3.3 V
Power Consumption	Slow (100 kHz) unbuffered	300 μ W per output
	Slow (100 kHz) buffered	800 μ W per output
	Fast (5 MHz) unbuffered	1 - 1.5 mW per output + 30 mW offset
	Fast (5 MHz) buffered	2.5 mW per output + 30 mW offset
Input Capacitance	Digital signals	< 4 pF
	Dsub, Vreset	Up to 50 nF (depending on detector and on reset mode)
	Vbiasgate	150 pF
	RefColbuf, RefSample	1200 pF
	Vnbias, Vpbias, Vncasc, Vpcasc	300 pF
	Vbiasoutbuf	10 pF
Special Features	Window mode	Direct addressing and reading of any rectangular sub-window
	Guide mode	Parallel operation of full field and window mode
	Scanning direction	Selectable in horizontal and vertical direction
	Output modes	1, 4 or 32 outputs
	Gain in fast mode	Adjustable from 1 to 16 in steps of 1
	Radiation hardness	Vertical scanner and internal mode selection registers are single event upset (SEU) proof